Dynamic Optical Adjustment of a PDV Signal in Real Time

Heather Leffler
Project Lead

Design Team: Adam Iverson, Araceli Rutkowski, Wendi Dresen, Jason Young

Sept 3, 2008

T100EEU042307

Project Background

Scope of Work:

This project will develop a control system to dynamically adjust the optical power of a PDV signal in real time.

Deliverable:

A prototype PDV unit that adjusts the optical power in real time to stabilize the signal-to-noise ratio of the PDV time domain data.

Benefits:

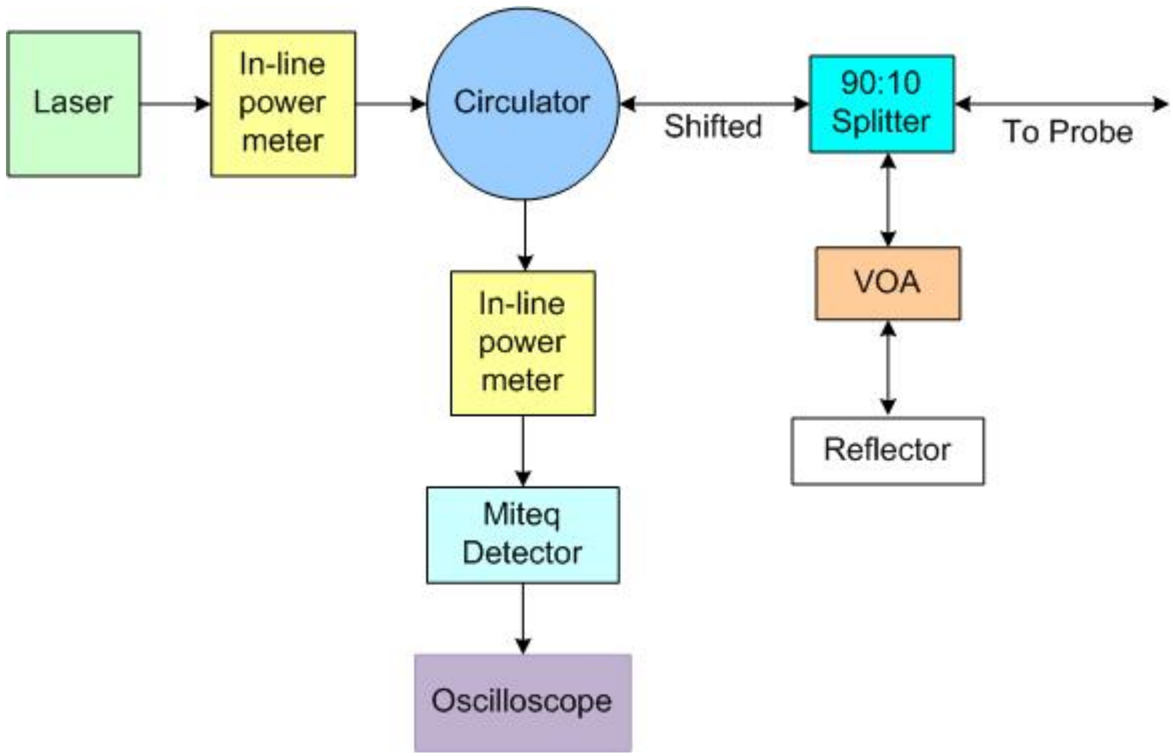
Dynamic optical signal adjustment stabilizes the signal-to-noise ratio of the time domain data, yielding a more consistent signal-to-noise ratio in the frequency domain data.

Project Motivation

- To increase the amount of data returned by a PDV system fielded on a dynamic experiment.
- When the beat amplitude drops below the noise floor of the detector, we lose frequency data, i.e. particle velocity data.
- A PDV system that can dynamically maintain the return signal amplitude within set limits can be fielded with only one oscilloscope channel per probe saving the cost of a second oscilloscope ($60K to $120K). *

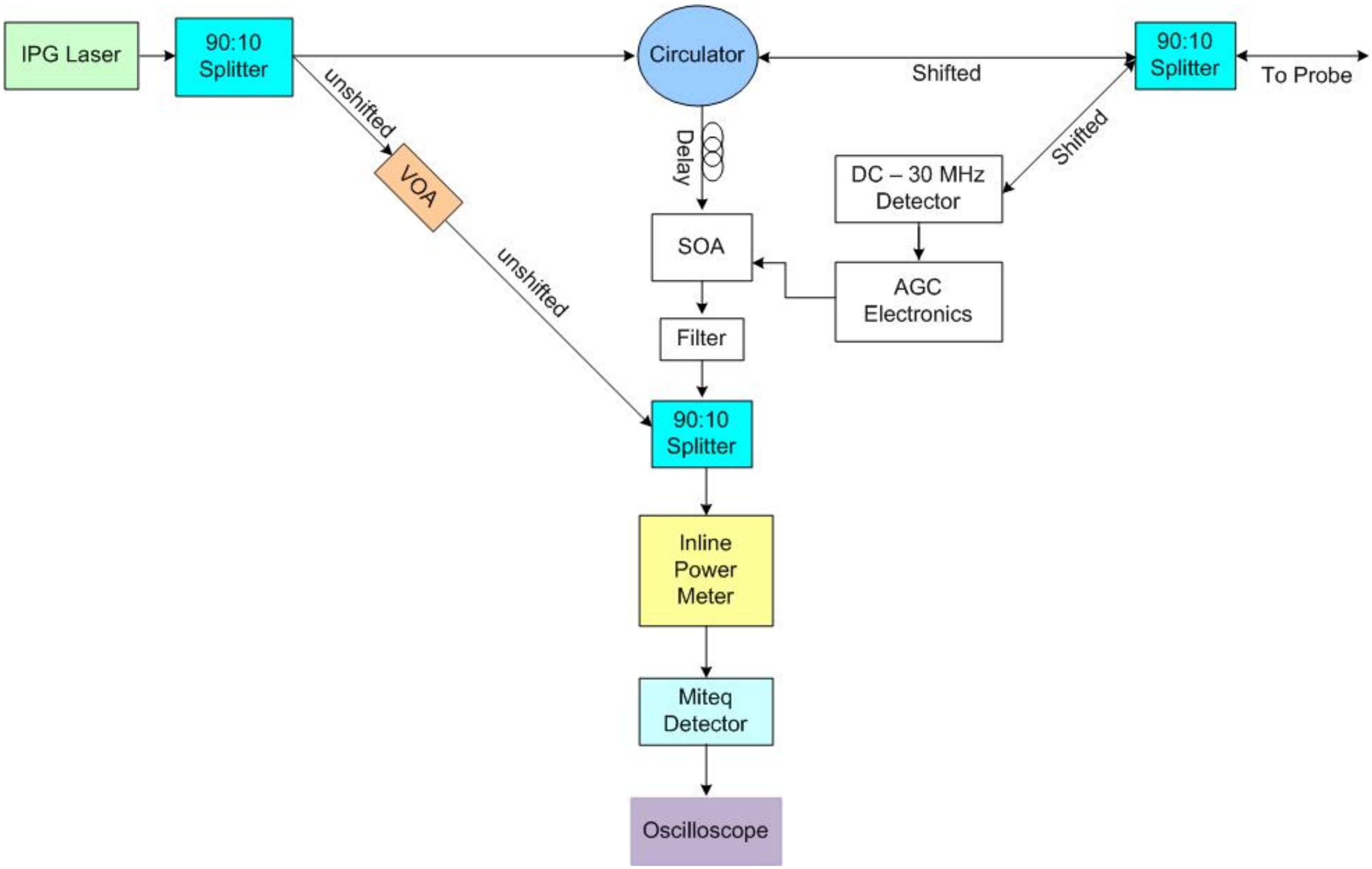
*Added benefit

Current LAO PDV Detector Module



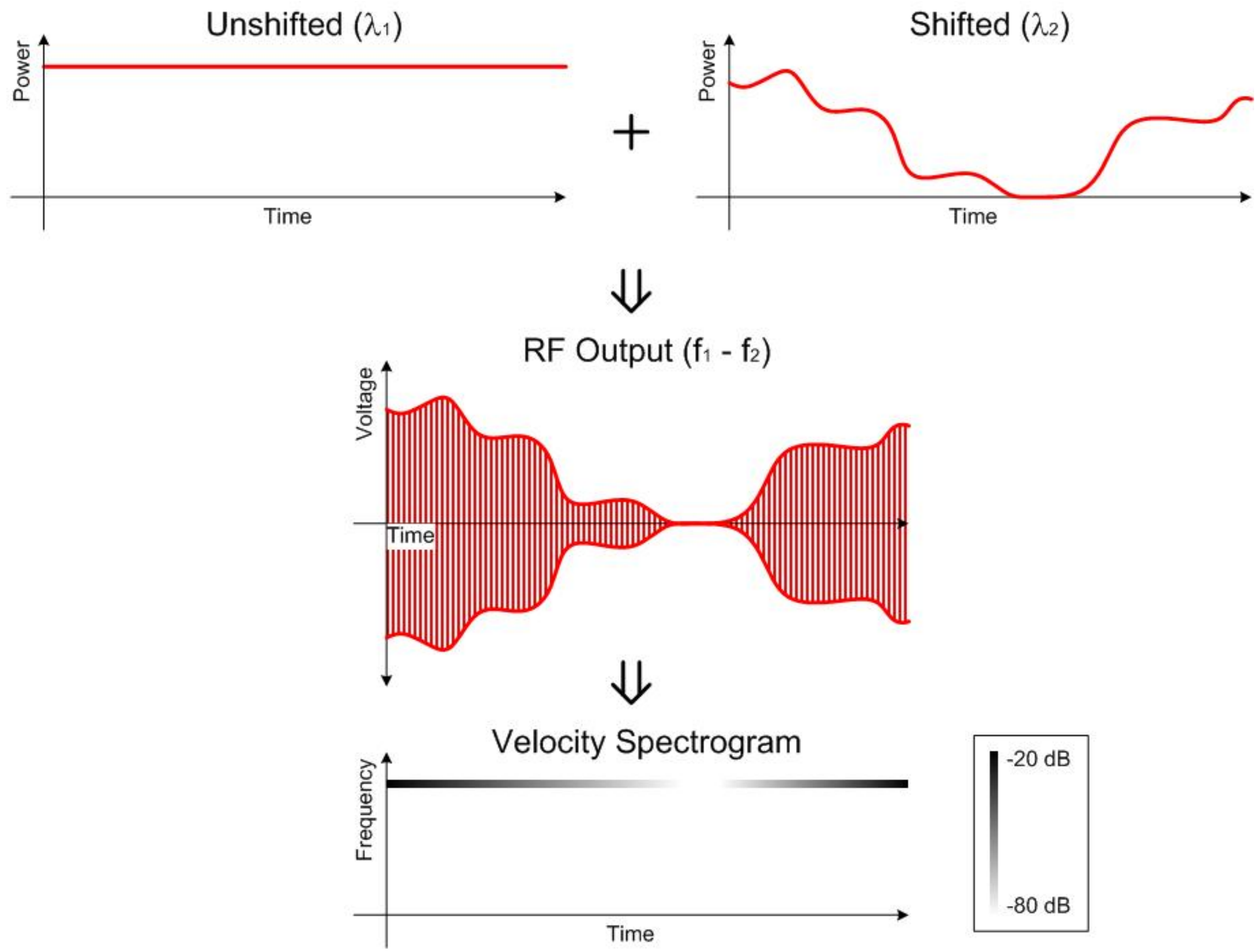
T100EEU042307

PDV System with Dynamic Optical Adjustment



T100EEU042307

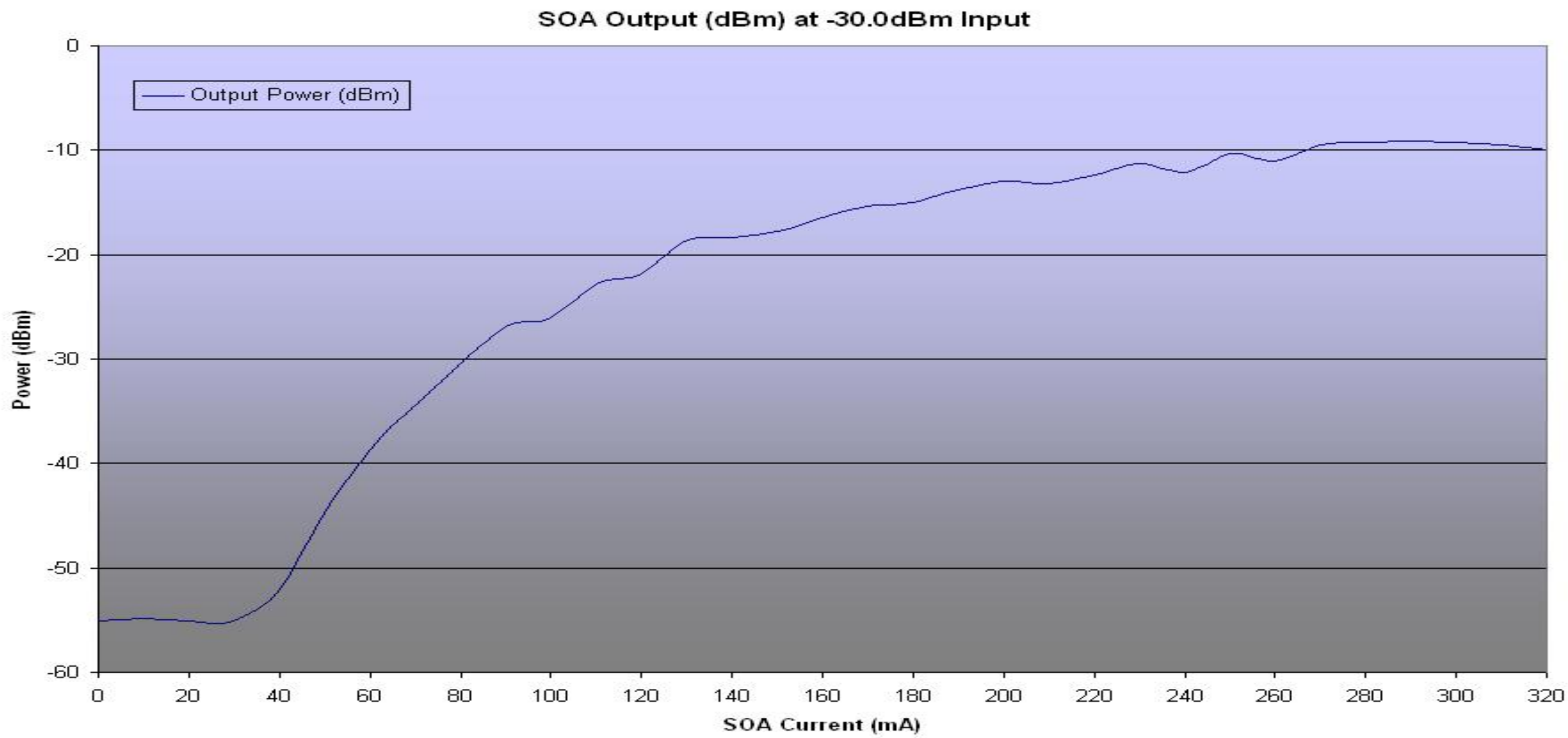
Simplified PDV Signal Problem



T100EEU042307

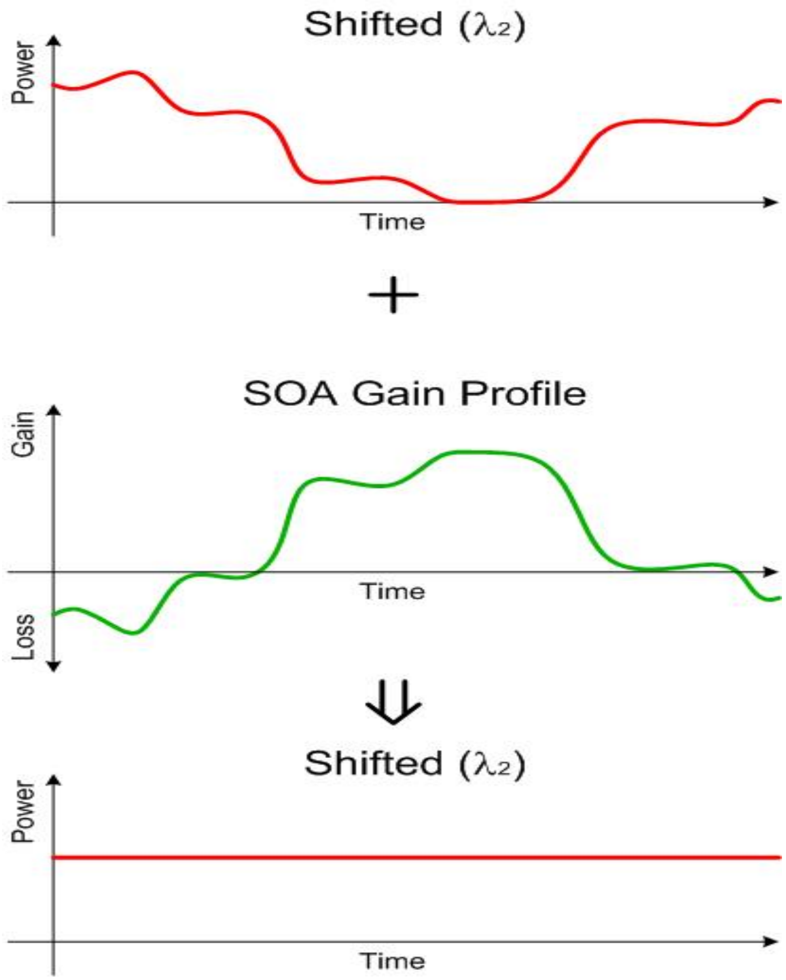
Semiconductor Optical Amplifier (SOA)

- Provides 15 dB of attenuation and 20 dB of gain.
- Response time is quoted at <100 ps.
- Current controlled from 40 mA to 250 mA.



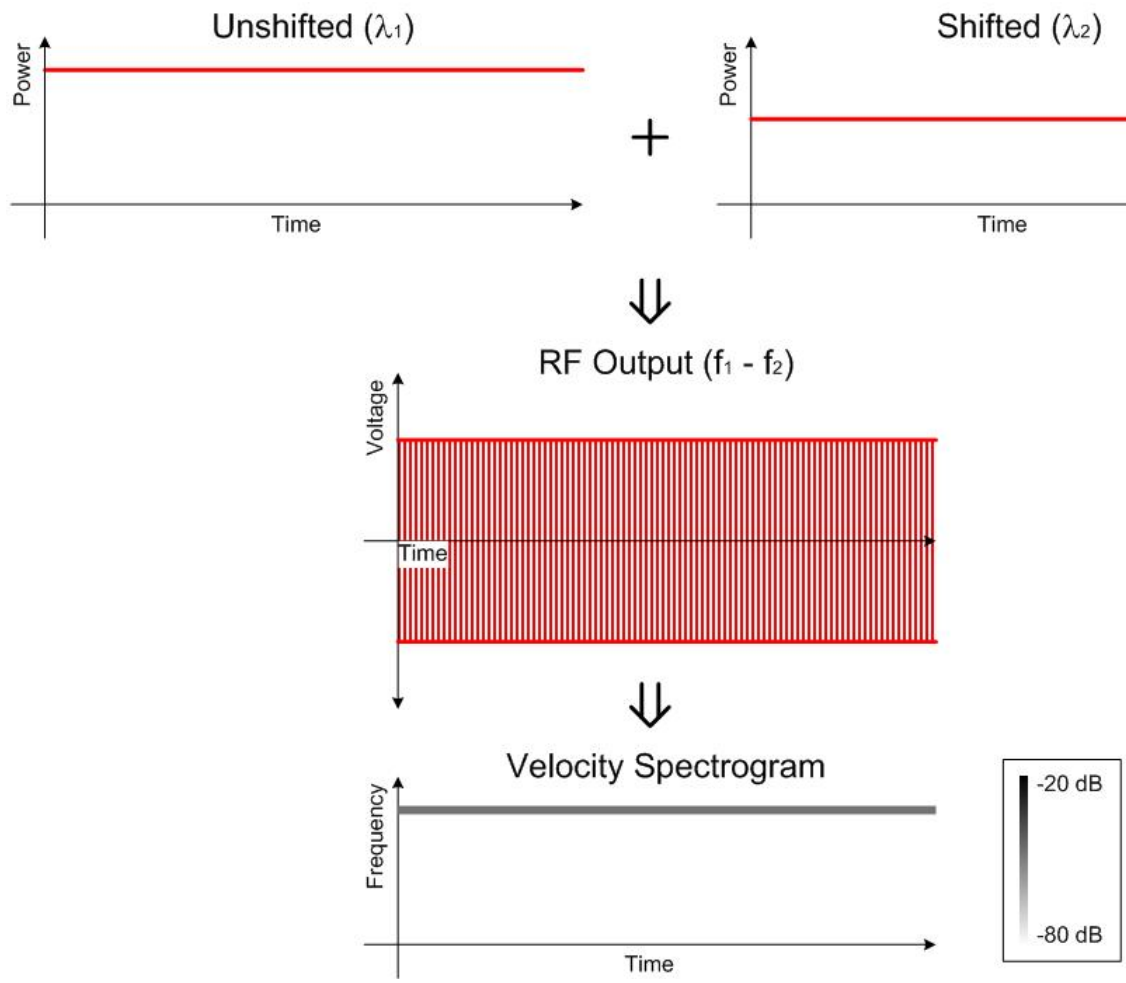
T100EEU042307

Proposed Solution – SOA used for both Gain and Attenuation



T100EEU042307

Proposed PDV Signal Correction



T100EEU042307

The Approach

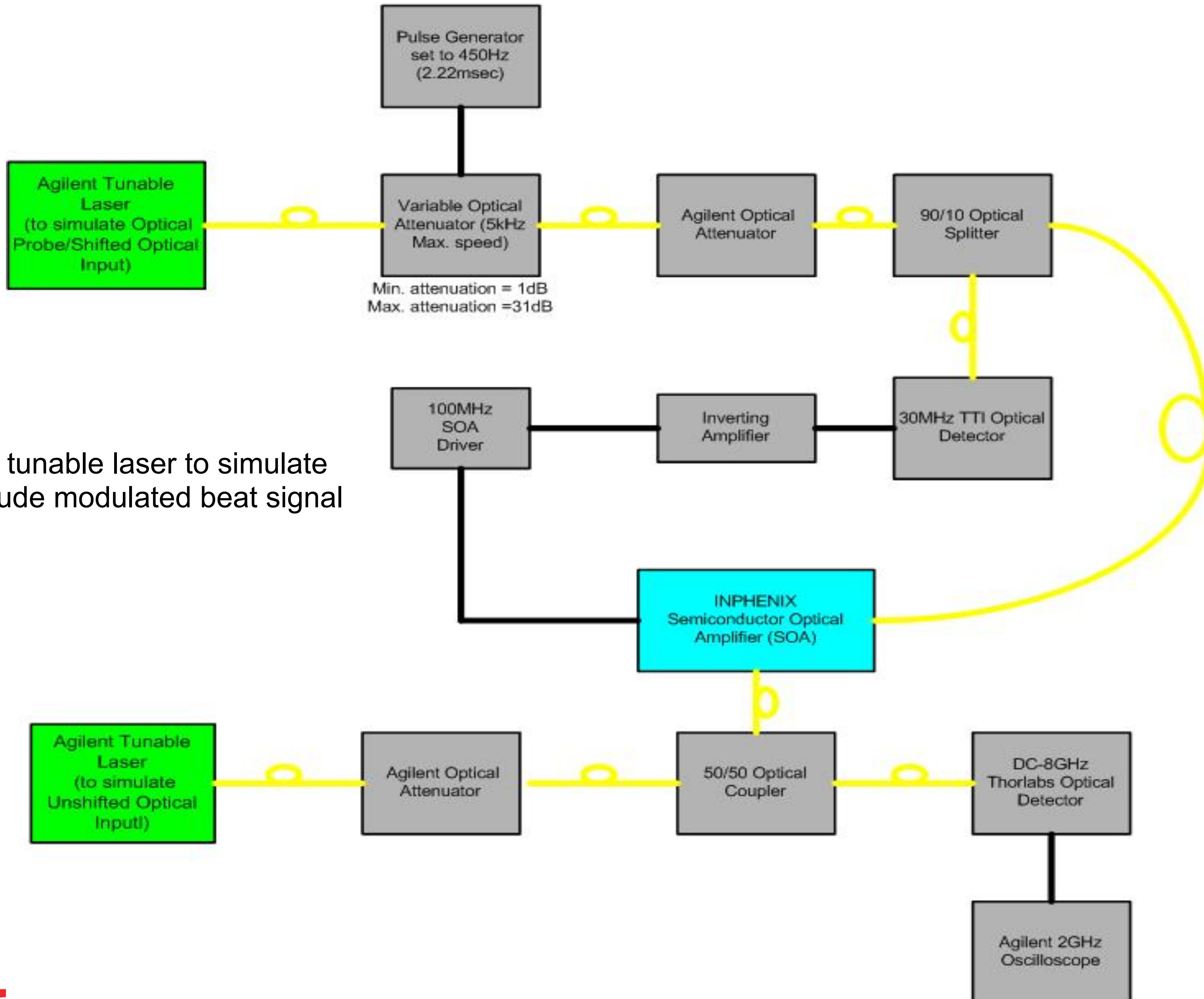
- Due to limited time and resources, decision to use only COTS evaluation boards – no time for a custom PCB.
  - Obtain an SOA and evaluate it.
  - Modify it's evaluation driver board to try to get more speed out of it.
  - Develop AGC circuits using COTS evaluation boards.
    - Digital AGC
    - Analog AGC

Digital AGC

- Used COTS FPGA evaluation board with on-board ADC and DAC.
  - Available selection of COTS evaluation boards with ADC and DAC on-board are too generalized for our needs – voltage levels are not a match, speeds not high enough. Chose the board that came closest to meeting our needs - Altera DSP Development Board, Statix II Edition with on-board 125 MSPS ADC and 165 MSPS DAC.
  - Thoroughly characterized the board and proved that a digital solution could work given careful component selection, electrical interfacing, and ADC/DAC matching.
    - Read a signal from the ADC into the FPGA using LVDS – ran it through a ROM lookup table and output it to the DAC via LVDS -> 160 ns system latency using 100 MHz clocking.

Analog AGC

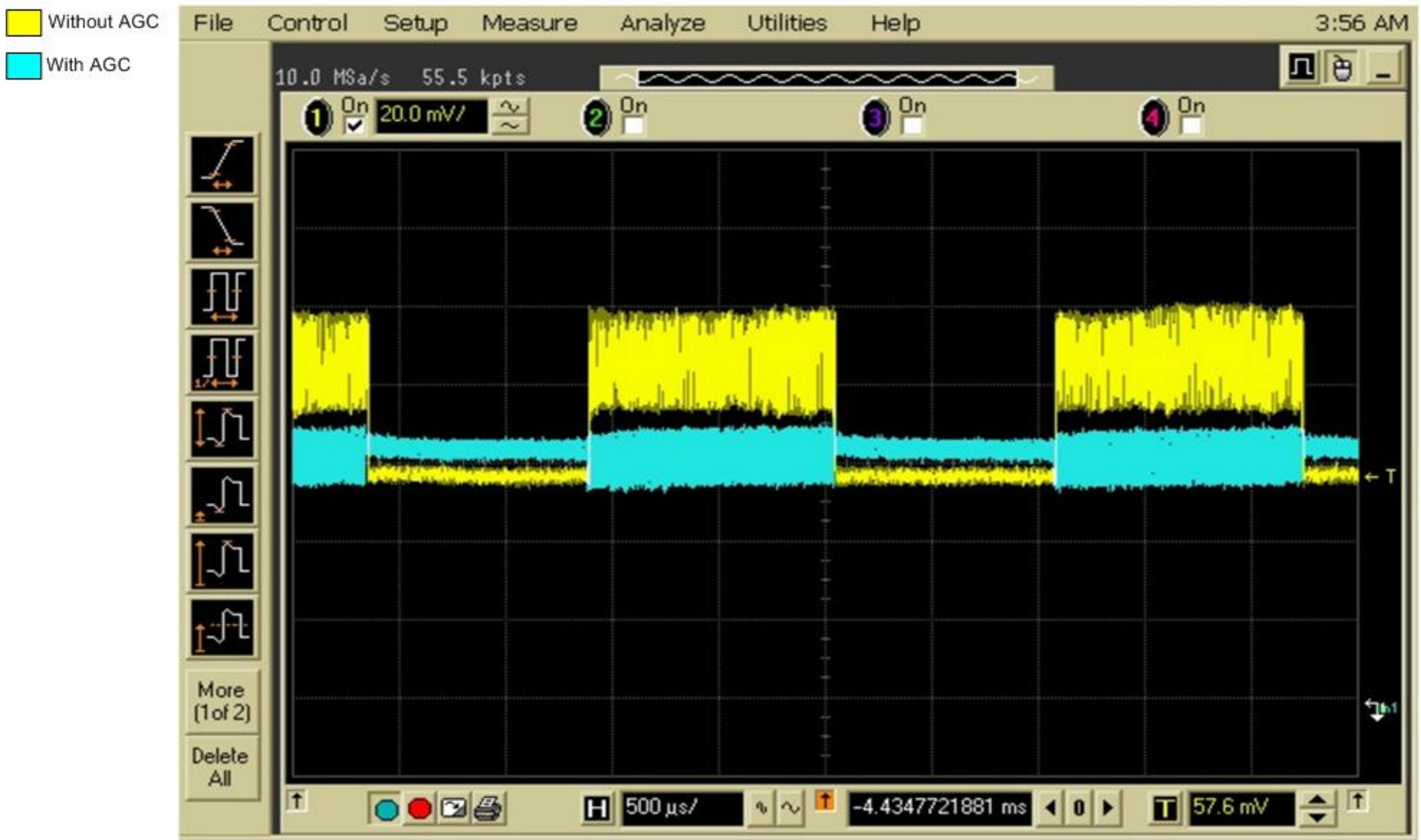
- Used two COTS Op Amp evaluation boards to create an inverting amplifier - drove the modified SOA evaluation board.
  - Higher speed version - tens of us of response time with 10 dB gain
  - Slower speed - 1 or 2 ms with 16 dB gain



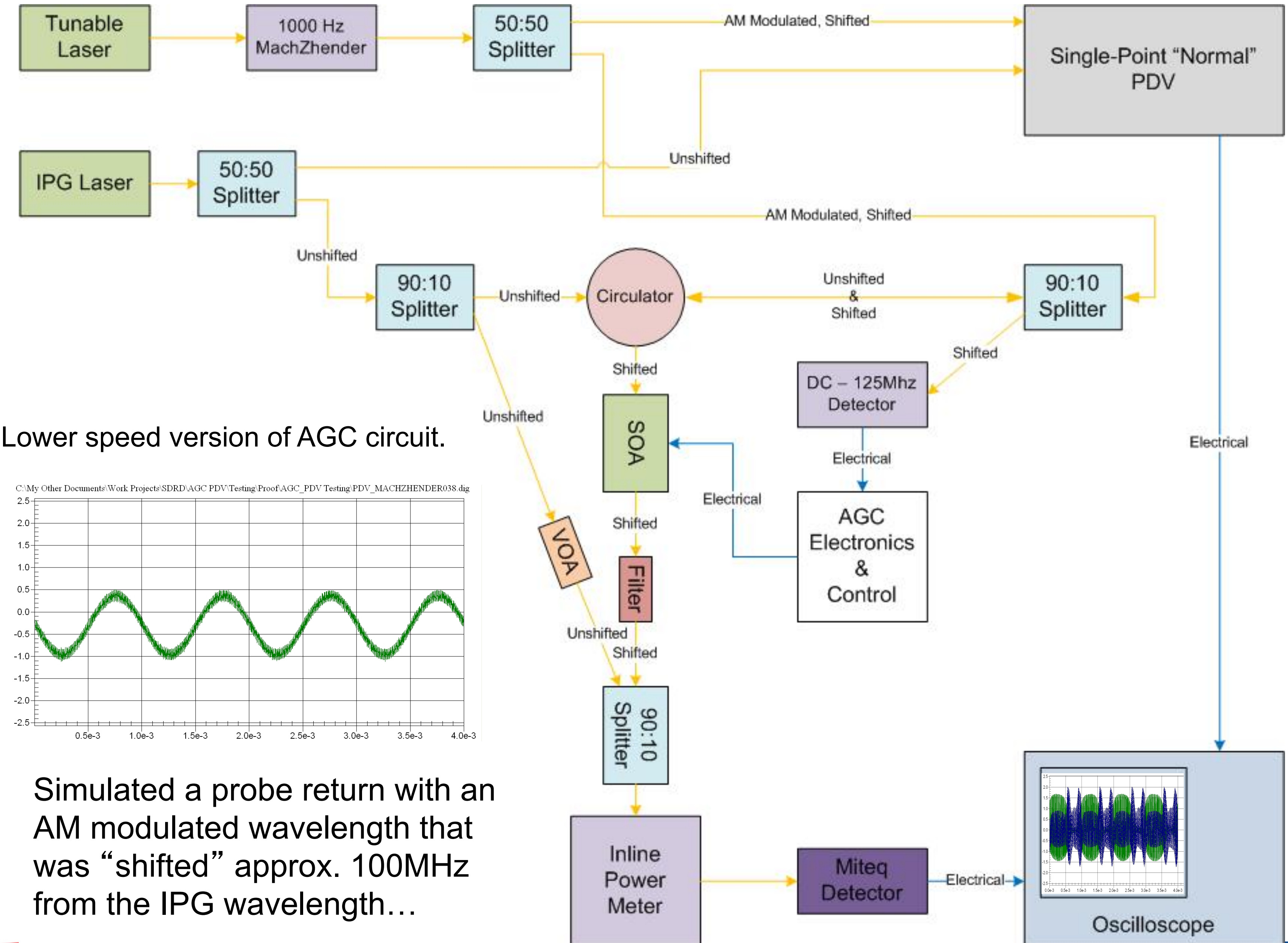
Used tunable laser to simulate amplitude modulated beat signal

T100EEU042307

With Probe Optical Power range into SOA = -15 to -45dBm



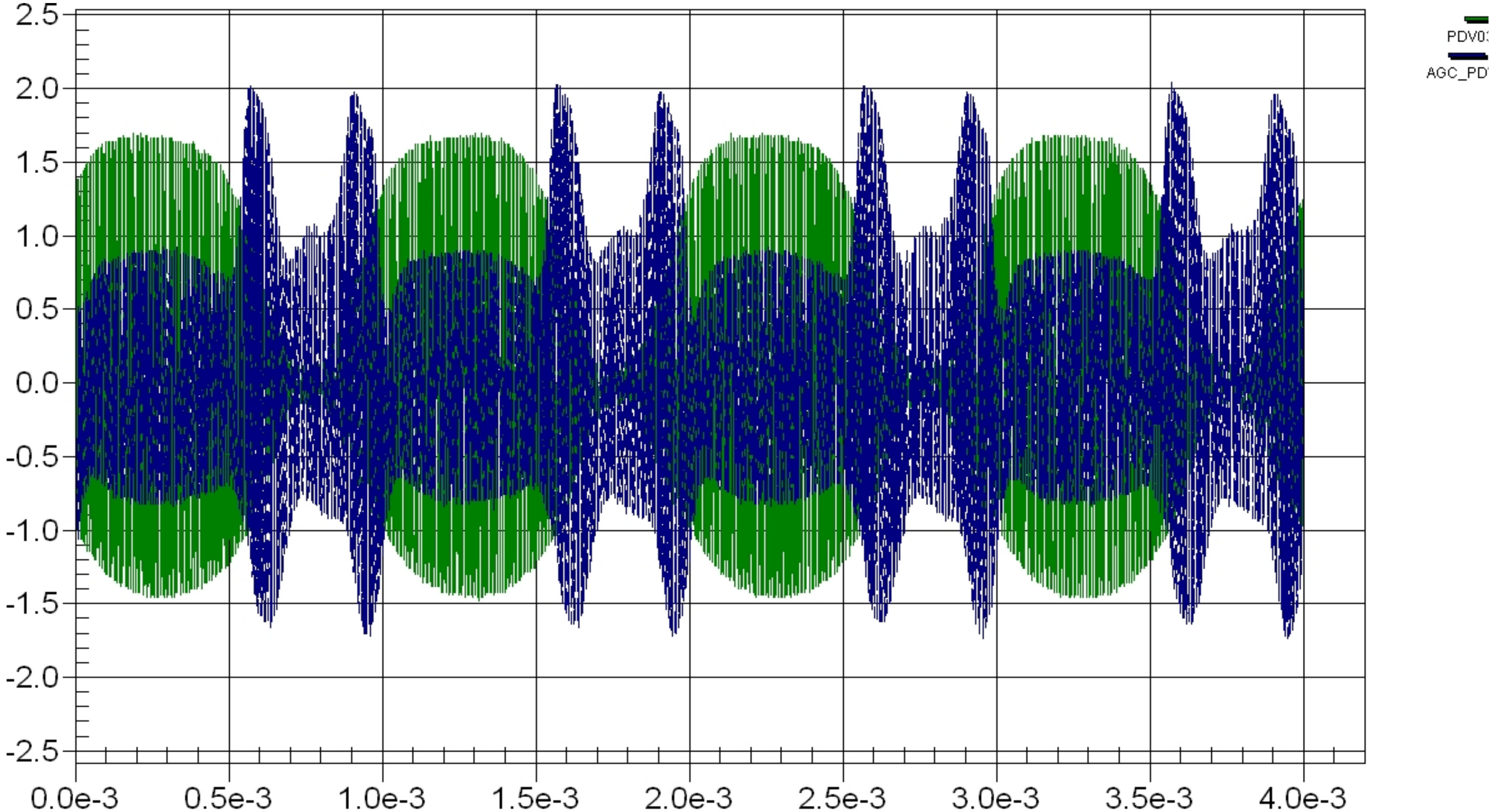
T100EEU042307



Lower speed version of AGC circuit.

Simulated a probe return with an AM modulated wavelength that was "shifted" approx. 100MHz from the IPG wavelength…

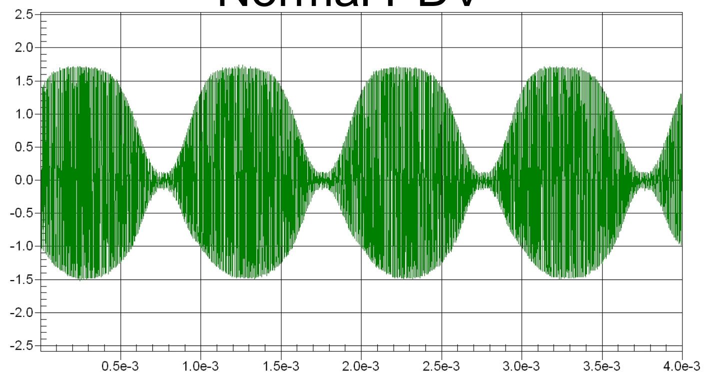
T100EEU042307

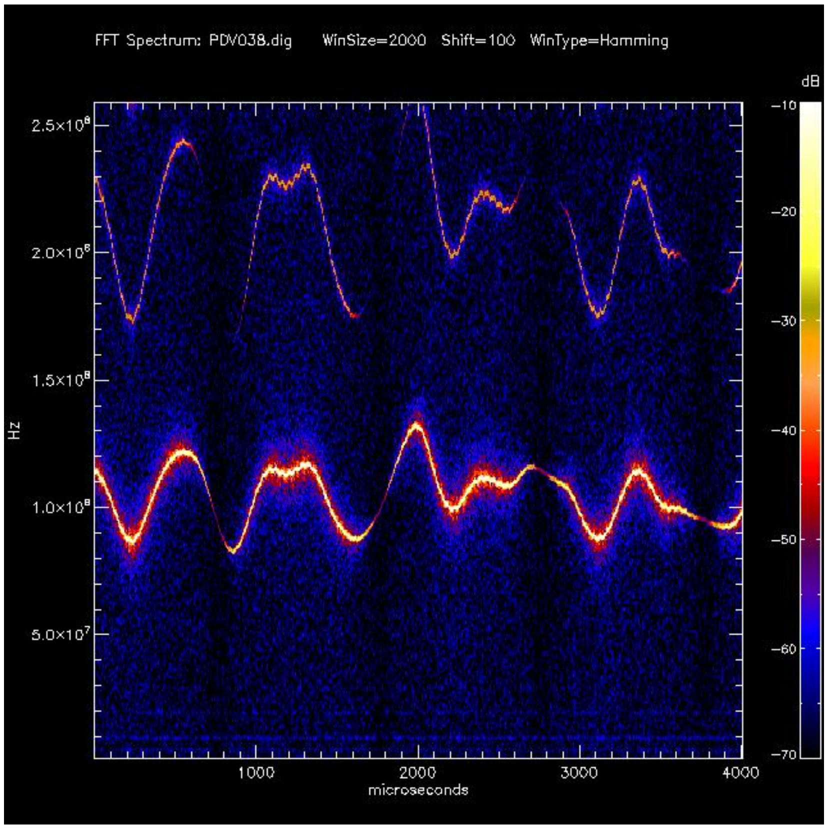


Green trace is normal PDV beat signal, Blue trace is AGC PDV beat signal…

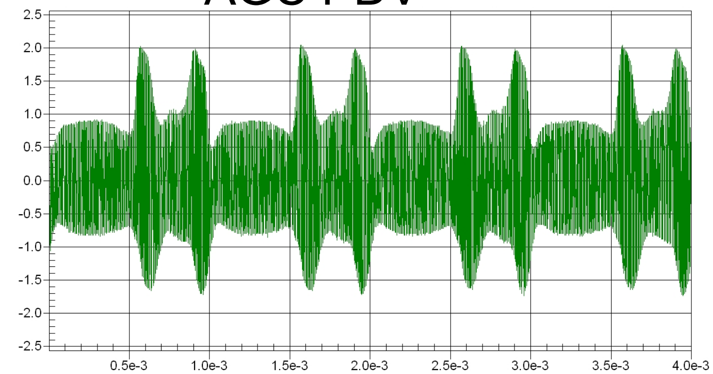
T100EEU042307

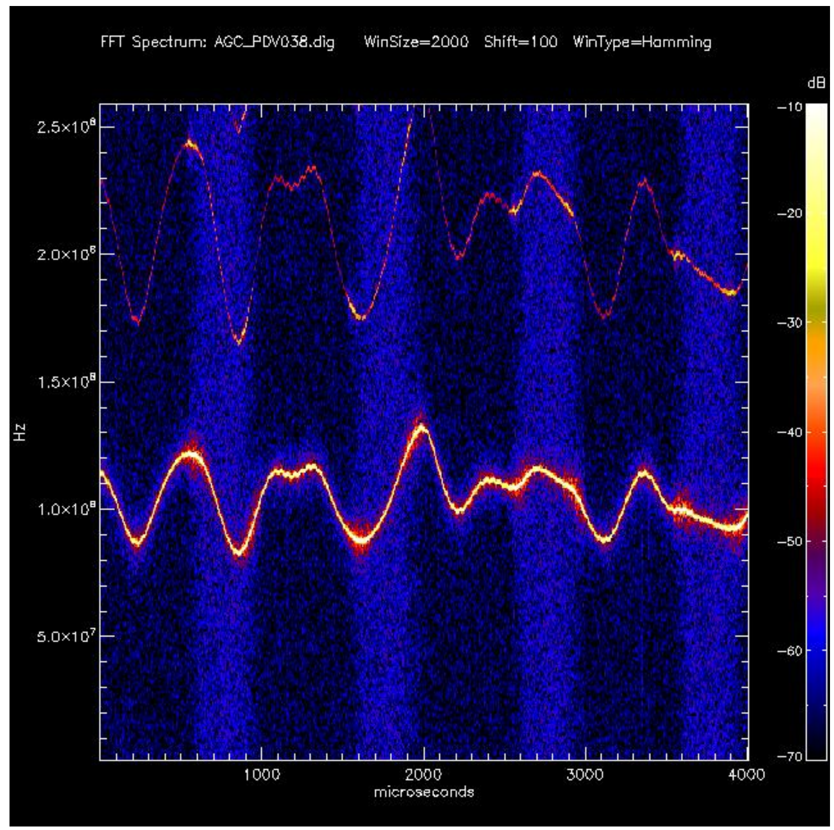
Normal PDV





AGC PDV





T100EEU042307

Summary

Demonstrated the ability to perform automatic gain control of a PDV signal in real time using an analog AGC circuit with 16 dB of gain correction and a response time of a few milliseconds.

Summary (continued)

- Determined that digital solution requires custom PCB.
- A custom design of the SOA driver circuit would allow us to meet our target speed of 100 ns and would also improve its linearity, thus reducing the output signal variation.
- Terahertz Technologies Inc (TTI) optical detector not sensitive below -30 dBm. Considering an APD for next year such as the Newport AD50APDir.
- Weren't able to do a dynamic test due to time constraints and the slower speed of our AGC, thus all of our data so far is lab simulated.
- We are looking for funding in FY09 to develop a much faster field ready prototype to stabilize the signal to noise ratio as well as constrain the dynamic range.