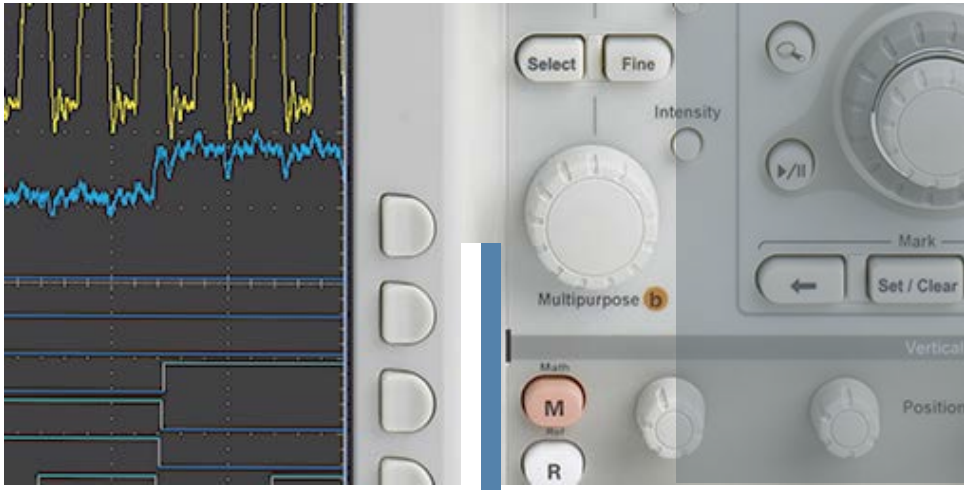
Real-time Oscilloscope Architectures

Dan Knierim, Tektronix Fellow



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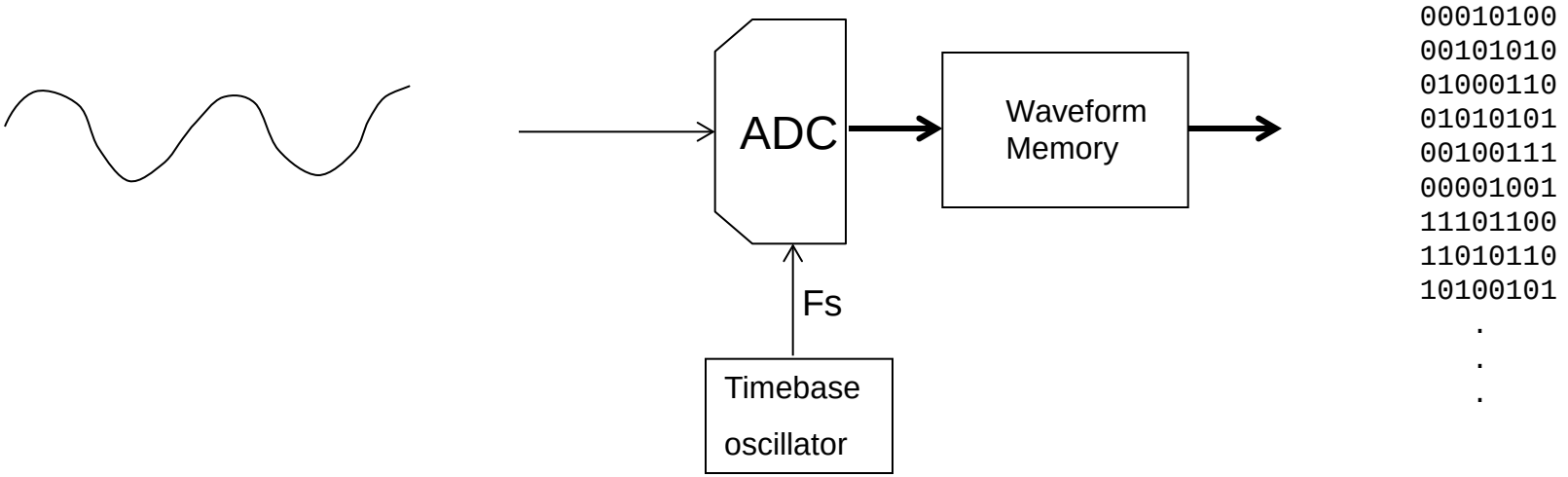
Simplest Architecture: Single ADC channel



Typical real-time ADC core speeds:

CMOS	0.1 to 1 GS/s
Bipolar	1 to 10 GS/s

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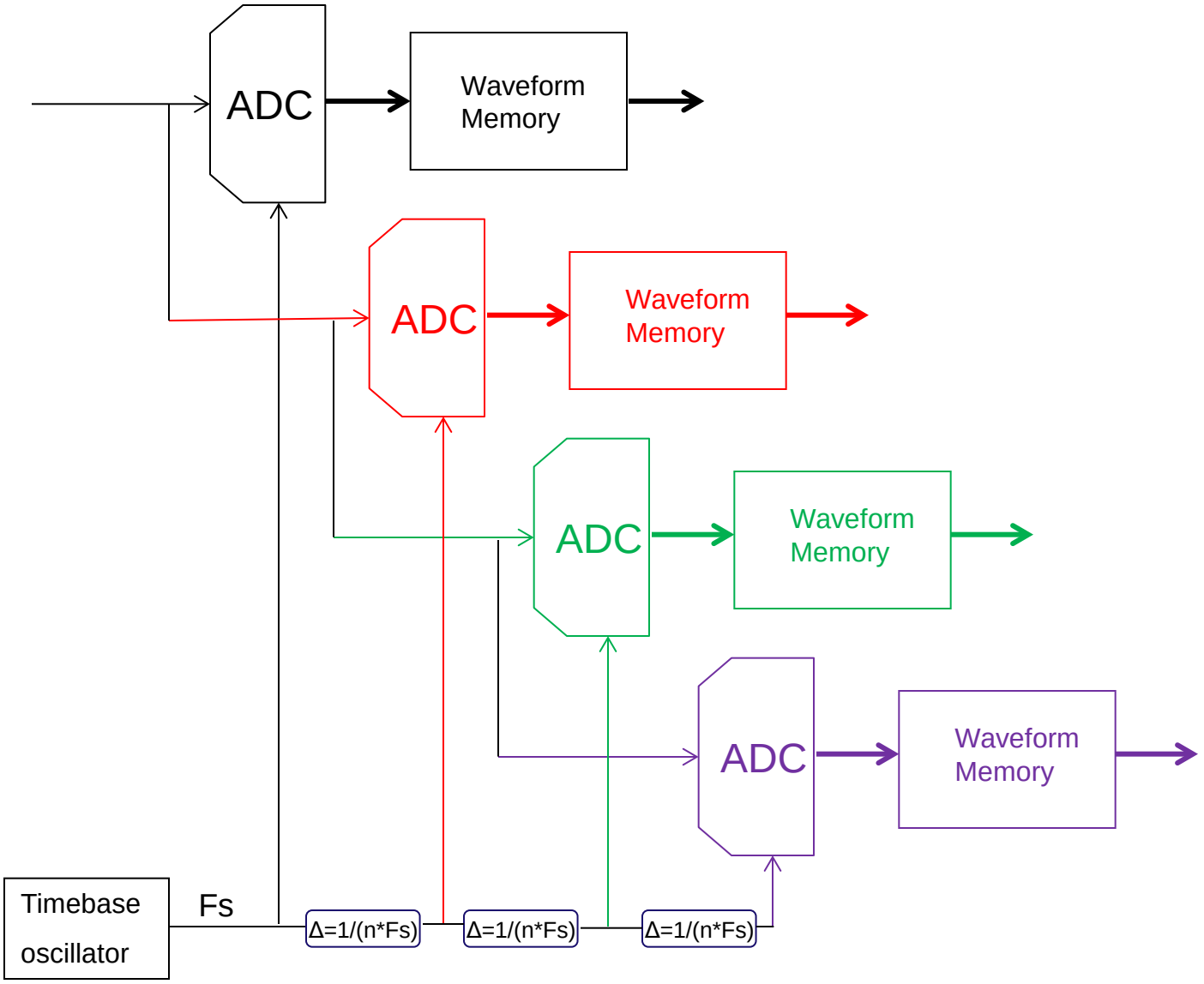
Multiple Time-Interleaved ADC channels



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Architectural trade-offs in acquisition performance

Performance Metric	N-way Interleaved
Sample Rate	N
Bandwidth	1
Record Length	N
rms Noise	1
Noise PSD	1/N
SFDR	↓
Effective Bits	↓
Phase linearity	---
Amplitude flatness	---
Price / Size / Power	~N

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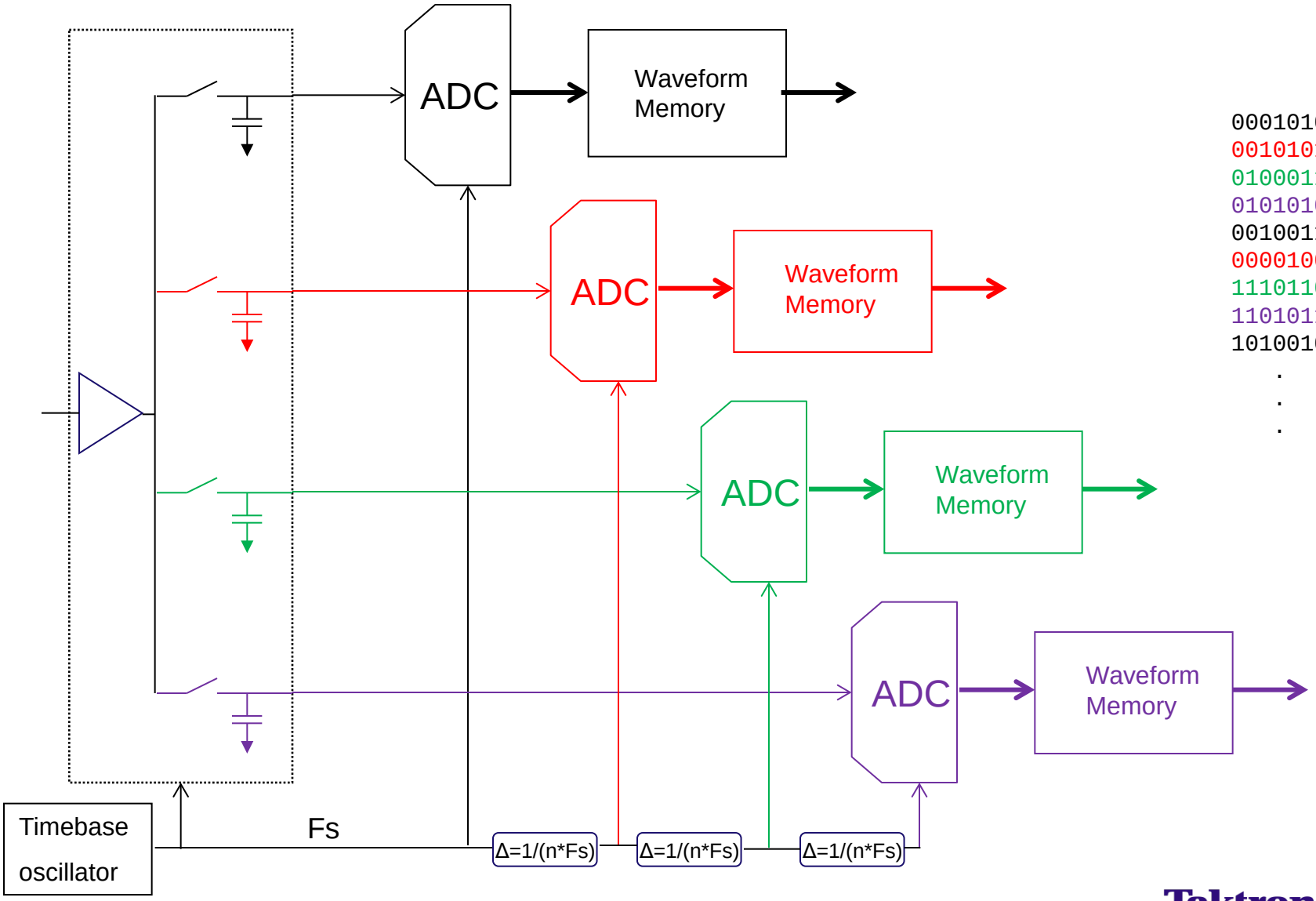
Multiple Pre-Sampled Time-Interleaved ADC channels



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Architectural trade-offs in acquisition performance

Performance Metric	N-way Interleaved	Pre-sampled Interleaved
Sample Rate	N	N
Bandwidth	1	W
Record Length	N	N
rms Noise	1	>1
Noise PSD	1/N	>1/N
SFDR	↓	↕
Effective Bits	↓	↕
Phase linearity	---	↑
Amplitude flatness	---	↑
Price / Size / Power	~N	>N

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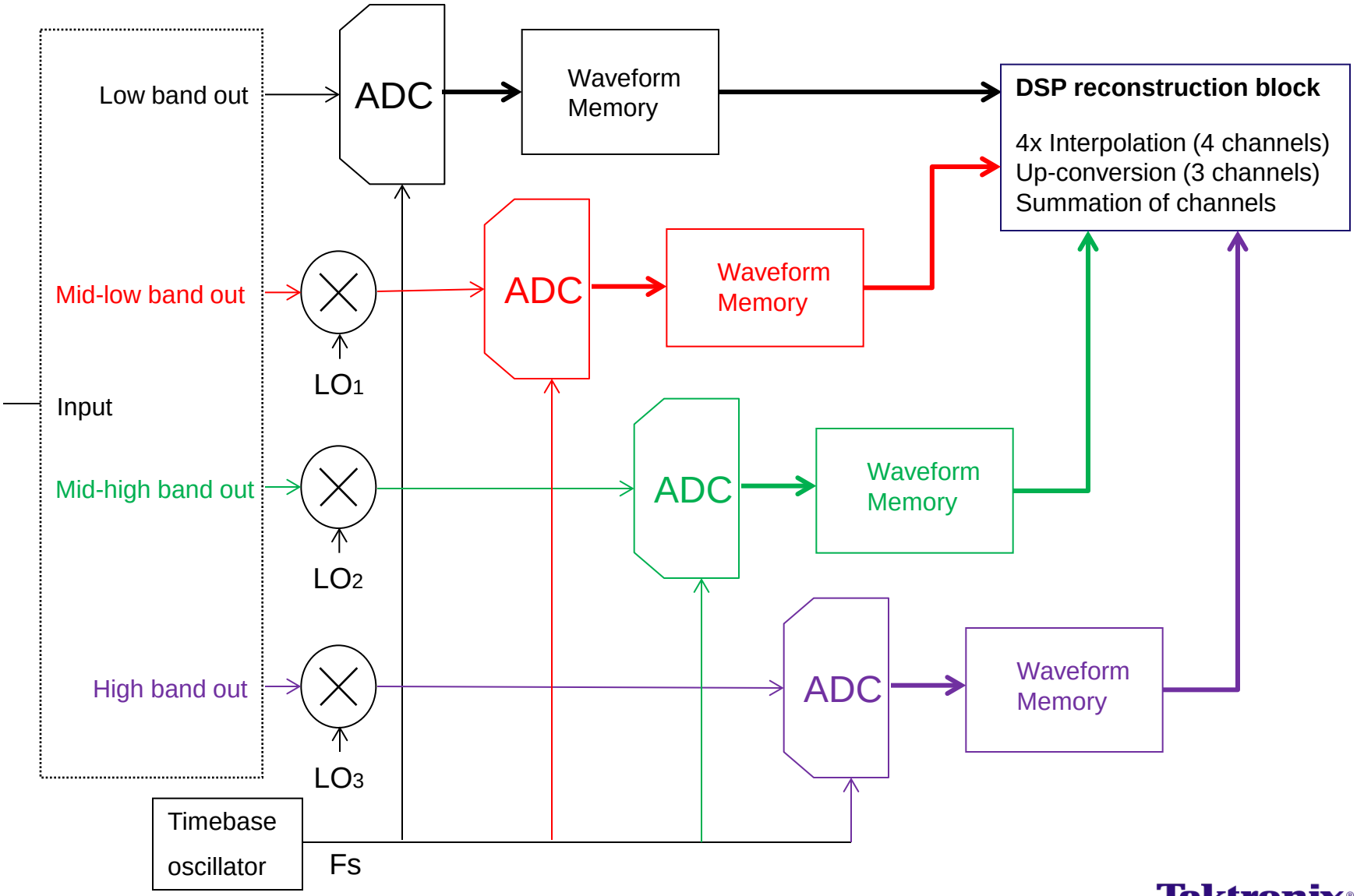
Frequency-Multiplexed (Band-Split) ADC channels



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Architectural trade-offs in acquisition performance

Performance Metric	N-way Interleaved	Pre-sampled Interleaved	N-way Band-Split
Sample Rate	N	N	N
Bandwidth	1	W	<N
Record Length	N	N	N
rms Noise	1	>1	$\sqrt{N}$
Noise PSD	1/N	>1/N	1
SFDR	↓	↕	---
Effective Bits	↓	↕	↓
Phase linearity	---	↑	↓
Amplitude flatness	---	↑	↓
Price / Size / Power	~N	>N	>N

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Architectural trade-offs in acquisition performance with DSP BW boost

Performance Metric	N-way Interleaved	Pre-sampled Interleaved	N-way Band-Split
Sample Rate	N	N	N
Bandwidth ↑	1	W	<N
Record Length	N	N	N
rms Noise ↑	1	>1	$\sqrt{N}$
Noise PSD ↑	1/N	>1/N	1
SFDR	↓	↕	---
Effective Bits ↓	↓	↕	↓
Phase linearity ↑	---	↑	↓
Amplitude flatness ↑	---	↑	↓
Price / Size / Power	~N	>N	>N
Overdrive Recovery ↓			

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Architectural trade-offs in acquisition performance with DSP BW limit

Performance Metric	N-way Interleaved	Pre-sampled Interleaved	N-way Band-Split
Sample Rate *	N	N	N
Bandwidth ↓	1	W	<N
Record Length *	N	N	N
rms Noise ↓	1	>1	$\sqrt{N}$
Noise PSD	1/N	>1/N	1
SFDR	↓	↕	---
Effective Bits ↑	↓	↕	↓
Phase linearity ↑	---	↑	↓
Amplitude flatness ↑	---	↑	↓
Price / Size / Power	~N	>N	>N
Overdrive Recovery ↓			

* Useful Sample Rate and Record Length are reduced at lower bandwidth settings due to data redundancy

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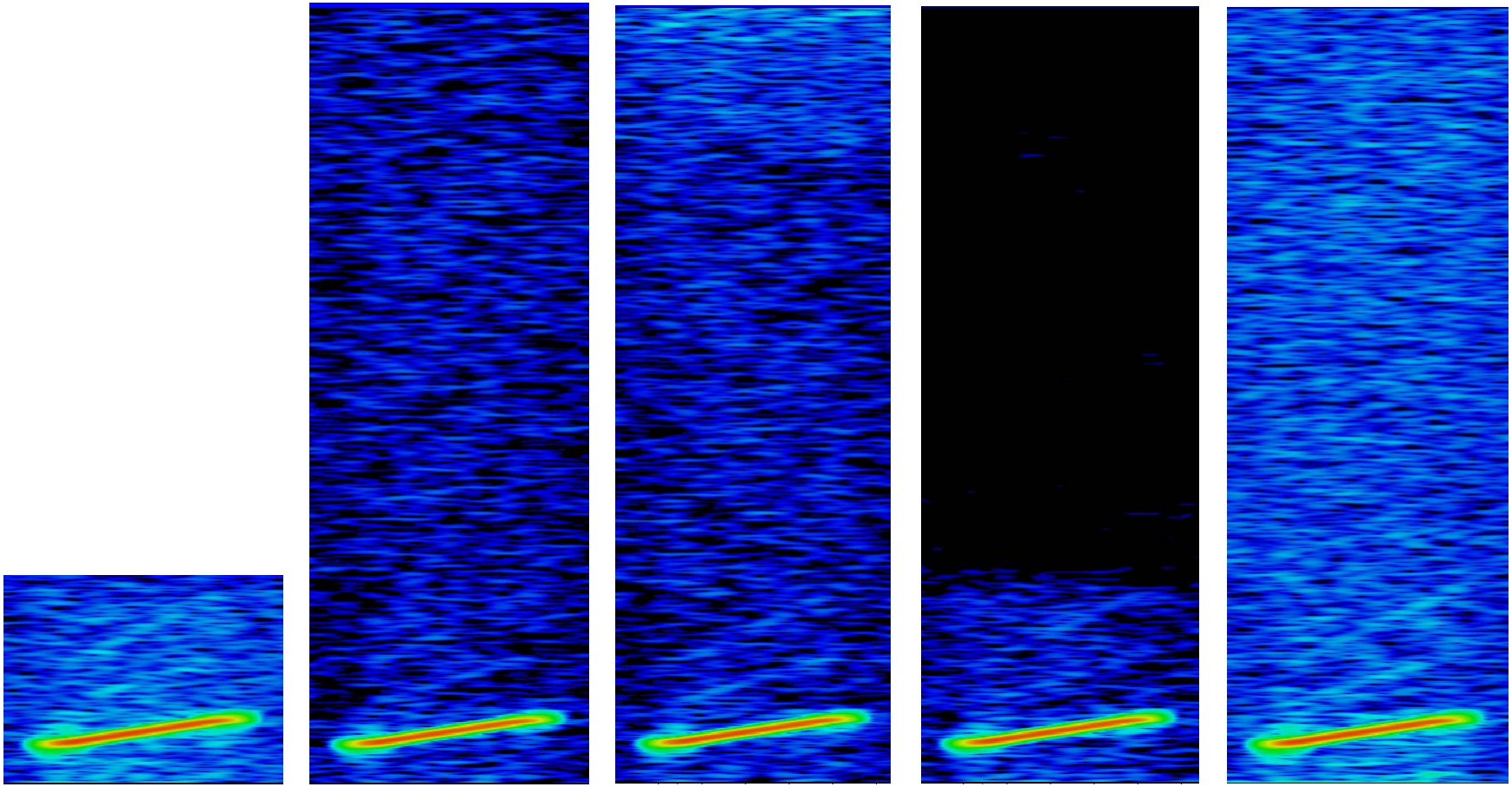
Architectural trade-offs: example spectograms



Single ADC channel

Pre-Sampled
4-way interleave

Pre-Sampled
4-way interleave
with DSP BW boost

Pre-Sampled
4-way interleave
with DSP BW limit

Simulation of
4-way band-split

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Conclusions

- Oscilloscope Architecture drives performance trade-offs
  - Straight Interleaving
  - Pre-sampled Interleaving
  - Band-splitting
  - DSP filtering

- It is fair to compare banner specs:
  - Sample Rate
  - Bandwidth
  - rms Noise (time domain)
  - Noise PSD (frequency domain)
  - SFDR
  - Effective Bits

- But don’t double-count benefits:
  - Sample Rate vs Noise PSD
  - DSP BW limit improves rms Noise, but not Noise PSD
    - Many frequency-domain analyses are sensitive to Noise PSD
    - Unexpected frequency content or amplitude spikes in single-shot experiments can be lost in the DSP

Questions???

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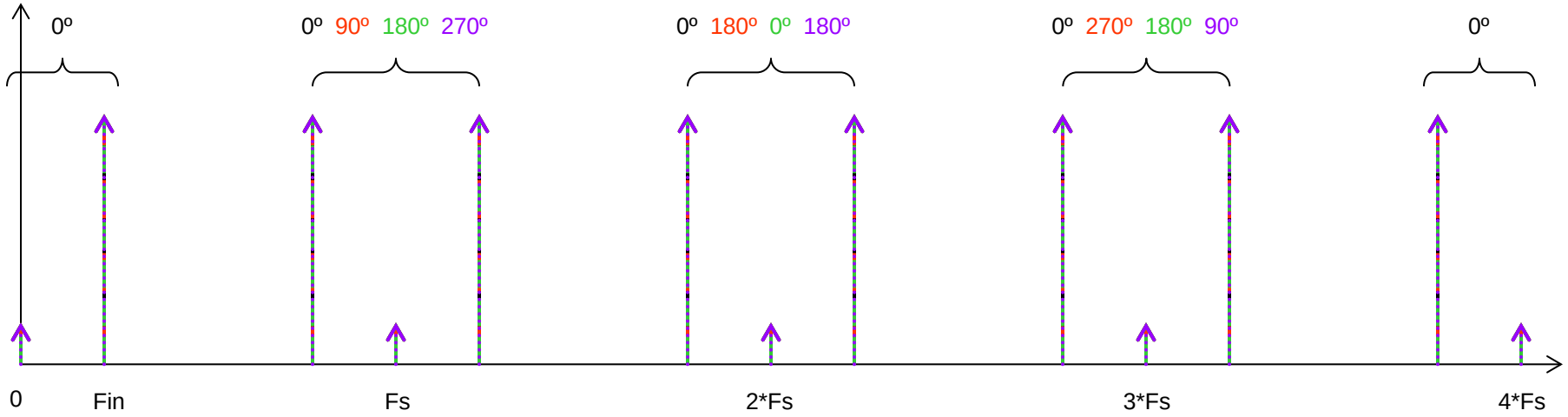
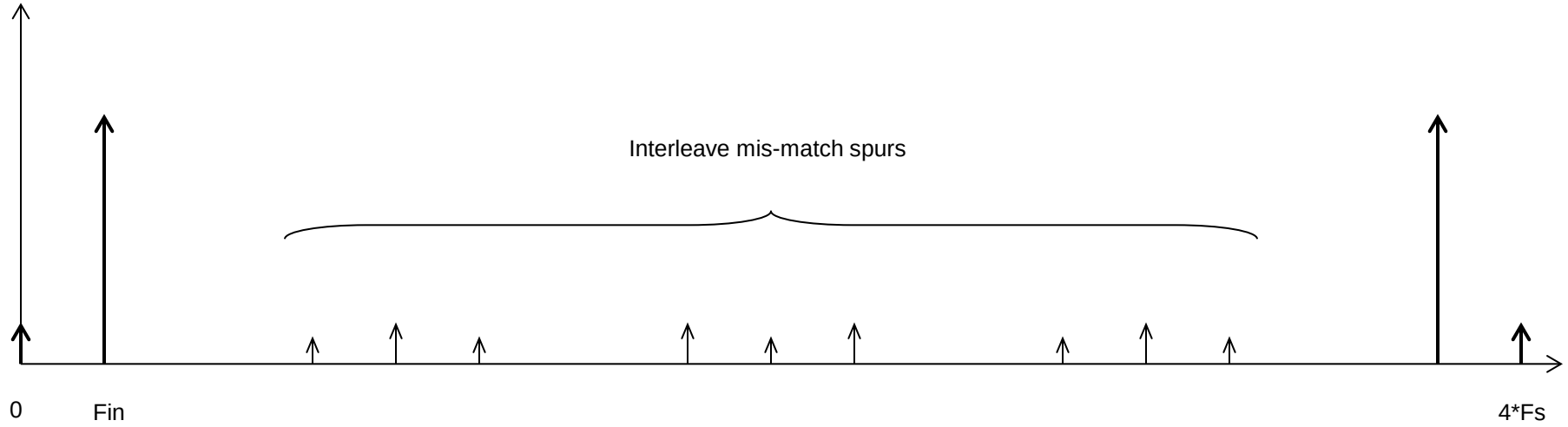
Interleaved Digitizer Architecture: mis-match spurs





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