Maximizing Digitizer Dynamic Range

Agilent Technologies

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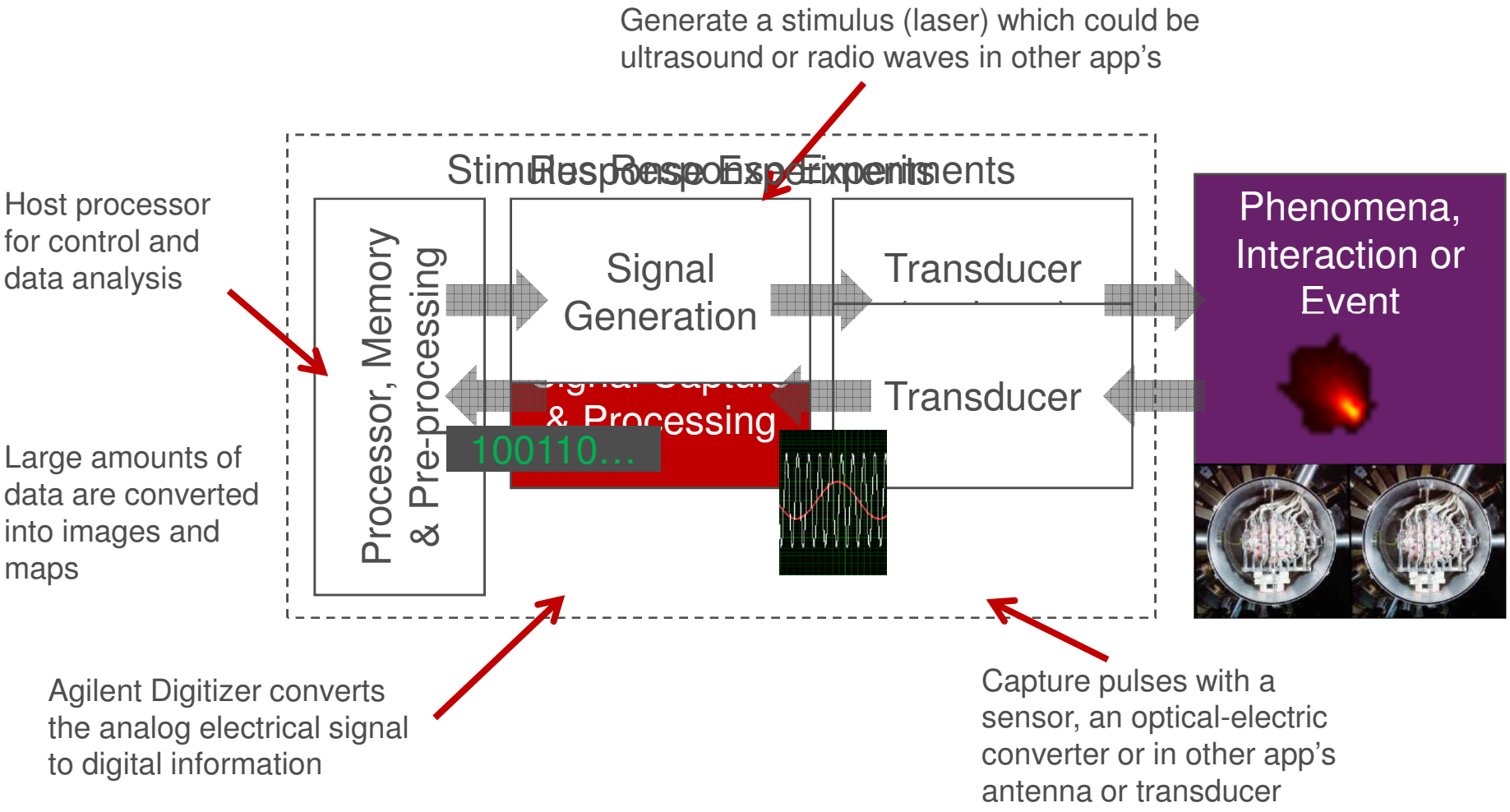
Agenda

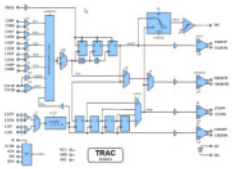
1. Introduction
   - Identifying a digitizer application
   - Block diagram overview
2. Dynamic range limitations
   - Analog to digital converter (ADC)
   - Front-end amplifier (FEA)
   - Clocking and synchronization
3. Increasing Dynamic Range
   - Channel stacking
4. Agilent State-Of-The-Art High Dynamic Range Digitizer
   - High-Speed Digitizer Technology Expertise
   - AXIe 12-Bit High-Speed Digitizer – See events that you could not see before

Typical Experiment or Measurement

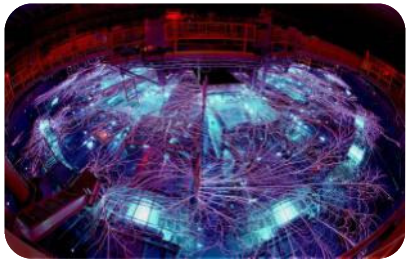


Size/power, speed, accuracy & lower cost of ownership

Achieving Single-Shot Acquisitions



ENOB
SINAD
SNR
THD
Thermal Noise
....



Installing Required Channels → **System Synchroniza-tion** → **Accurate Measurement** → **Data Storage** → **Operational Software**

- Integrate into 2, 5 or 14 slot chassis
- Synchronize >80 ch

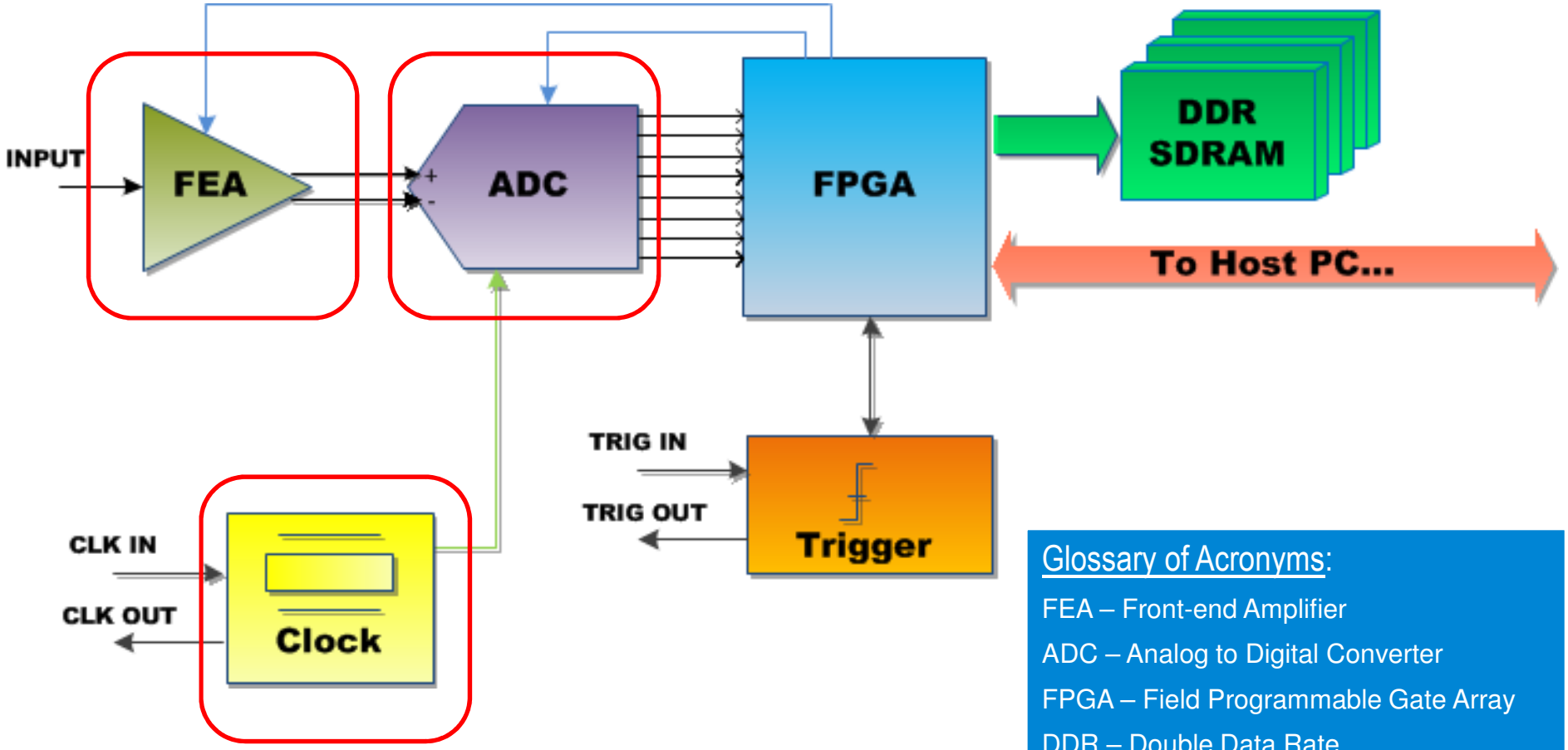
- Backplane local bus
- External clocking schemes
- Trigger time interpolation

- Beyond banner specs
- Taking all sources of error into account

- Large memories
- Data recording
- Battery backup

- Management of system configuration
- Data acquisition safety
- Fail-safe operation

Simplified One-Channel Digitizer Architecture



Glossary of Acronyms:

FEA – Front-end Amplifier

ADC – Analog to Digital Converter

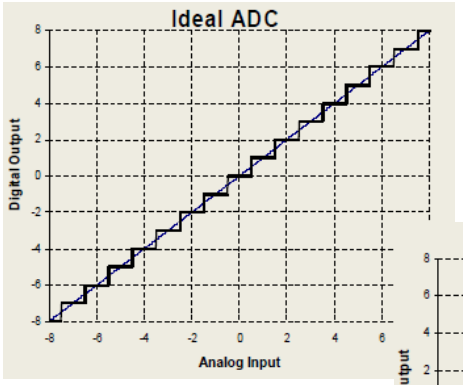
FPGA – Field Programmable Gate Array

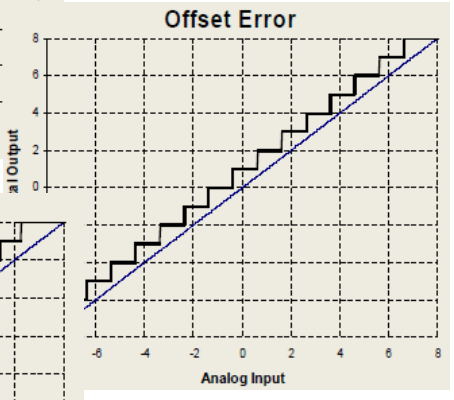
DDR – Double Data Rate

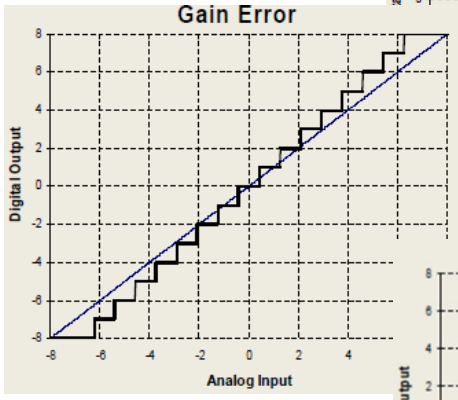
SDRAM – Synchronous Dynamic Random Access Memory

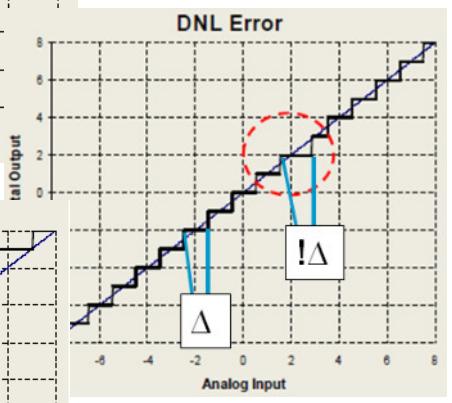
ADC – Analog to Digital Converter

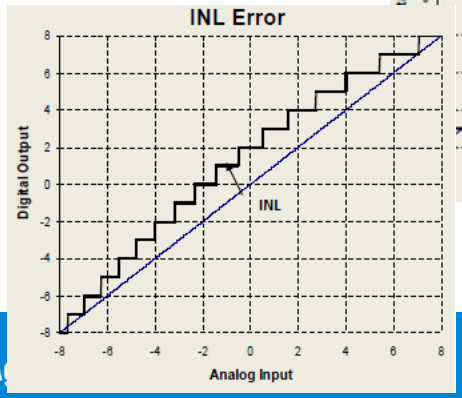
- Ideal ADC
  - Input is quantized into uniform steps
  - Transitions at +/- 50% of Δ
  - Discretely spaced samples at an infinite sampling rate
- ADCs have their own errors/performance
  - Offset/gain error
  - INL/DNL
  - ENOB, SNR, SFDR
  - …
- Digitizer design needs to maximize ADC performance



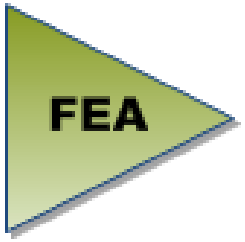






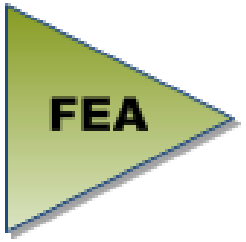


FEA – Front-end Amplifier



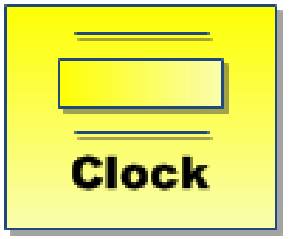
- Banner specifications
  - Offset range (example: +/-2*FSR)
  - Full scale range (example: 1V, 2V, etc.)
  - Input impedance (50Ω / 1MΩ)
  - Input coupling options (DC/AC)
  - 3dB analog bandwidth
  - Bandwidth limit filter (BWL)
  - Frequency response flatness (e.g. +/-1 dB)
- Design challenges – Sources of error
  - Reach wide bandwidth with DC coupling and high dynamic range
  - Large input DC offset
  - Good circuit protection
  - Whilst limiting the addition of noise and distortion

FEA – Challenges



- Reach wide bandwidth with DC coupling and high dynamic range
  - ADC inputs are usually differential, while digitizer inputs need to be single-ended → Requires a single-to-differential circuit
  - Single-to-differential circuit is usually either
    - a) BALUN → No distortion added
      → Difficult to have DC coupling; bad DC to AC behavior
      → Can be quite high band
    - b) Amplifier → Adds distortion
      → Easy DC coupling
      → Difficult to reach wideband
- Large input DC offset
- Good circuit protection
- All of that and still limiting the addition of noise and distortion
  - Components add thermal noise
  - Active components add distortion

Clock Creation and Distribution



- Banner specifications:
  - Added sampling jitter (example: 225 fs nominal)
  - Clock accuracy (example: ±1.5 ppm)
  - Clock modes (internal/external reference, etc)
- Design Challenges:
  - Minimize the added jitter to not deteriorate ADC performance
  - Distribute clocks precisely for synchronization across channels
  - Immunity to perturbations (high speed clocks)

Influence of Sampling Clock on Digitizer Performance

- ADC Maximum Reachable theoretical SNR (no distortion):

$$ENOB = \frac{SINAD\ - 1.76}{6.02}$$

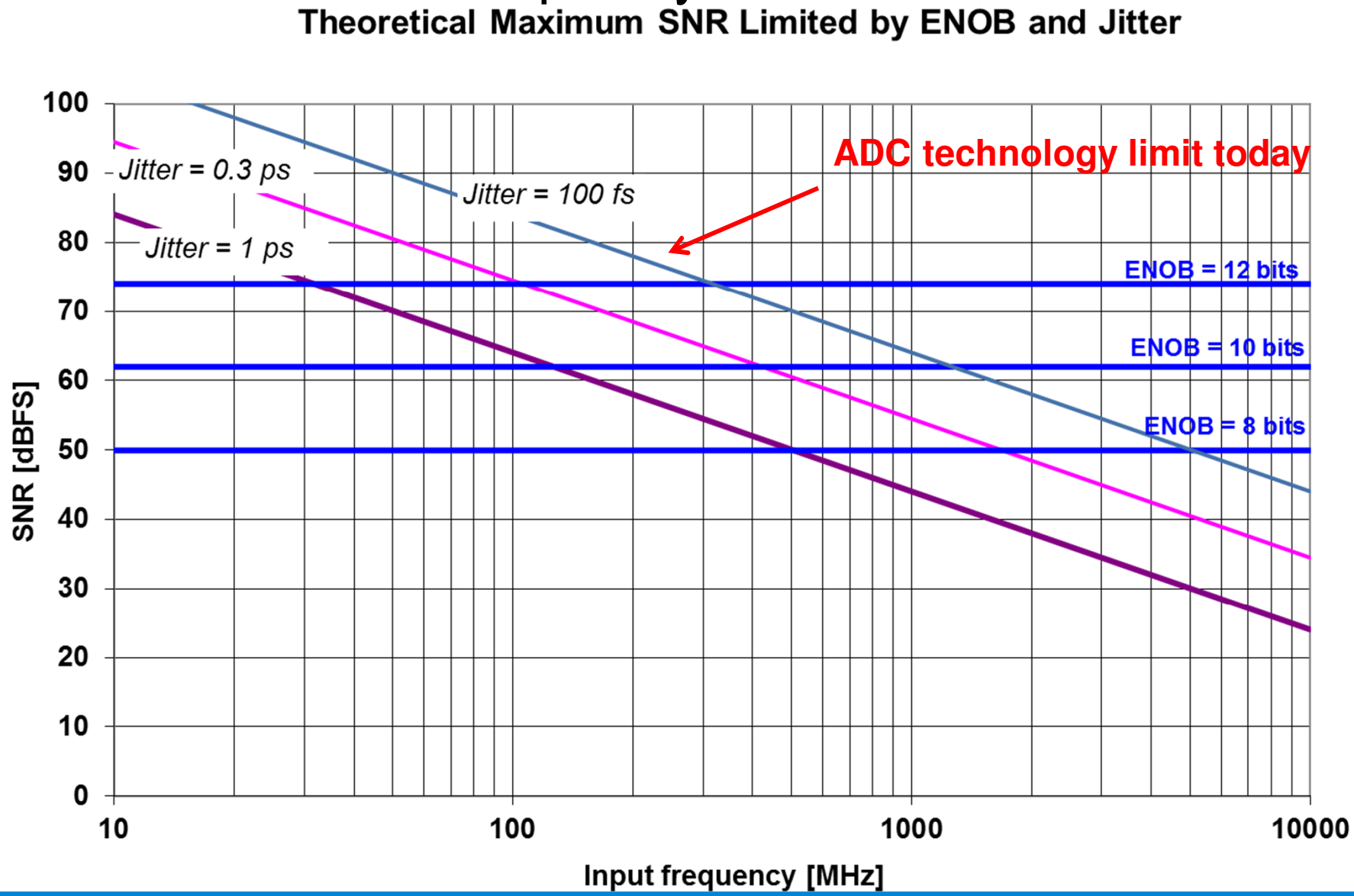
$SINAD$ = S/(N+D) = SNR, when no distortion

$$\rightarrow \text{SNRmax} = (\text{Resolution x } 6.02) + 1.76$$

- Sampling jitter also limits the maximum reachable SNR in function of input signal frequency

$$\text{NOISEmin} = -20\text{xlog}(2\boldsymbol{\pi} f x Jitter)$$

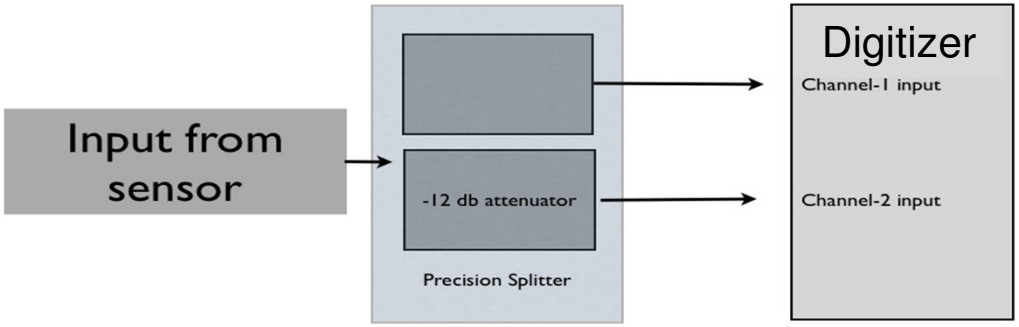
SNR & ENOB vs. Frequency



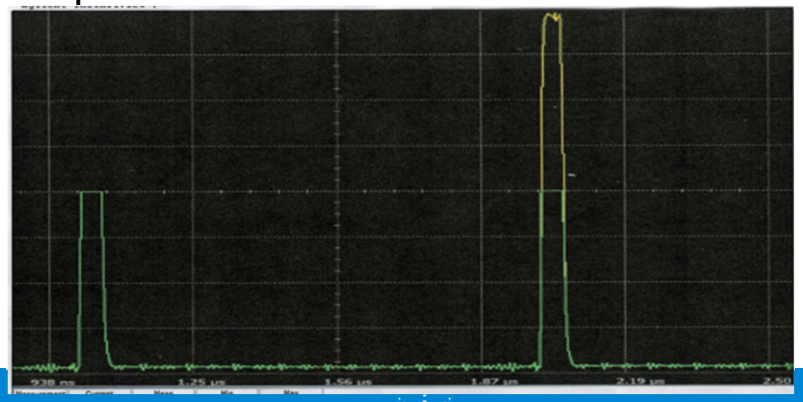
How To Maximize Digitizer Dynamic Range?

- Increase ADC resolution
  - In the GHz area experiments traditionally use 8-bit ADCs with ENOB of approximately 6-7 Bits
  - State-of-the-art is now 12-bit → Design challenges are stronger!
- Processing techniques
  - E.g. averaging
  - Limited by sampling rate – again trade-off resolution/speed
- “Stacking” channels to increase the resolution
  - Requires very good channel-to-channel synchronization
  - Requires large DC offset ranges

Channel “Stacking”



- A pulse is launched through a precision 50 ohm splitter
- One path goes directly to an input channel
- The second path is attenuated. In this case the amplitude is reduced to 25 % of the first path (-12dB). Use a more sensitive full-scale-range on Ch2 of the digitizer
- Change channel DC offset for “stacking” the channels → the input signal can be larger than a single window and the second channel will then record the over signal, and increase the number of quantization levels

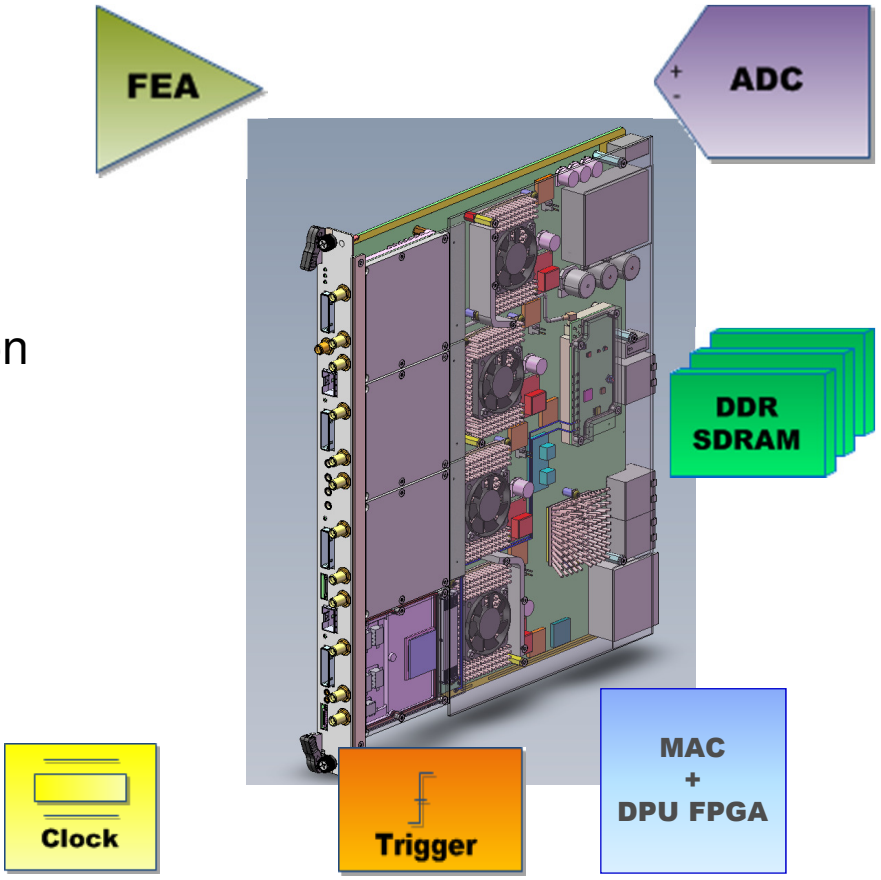


Agilent High-Speed Digitizer Technology Expertise

A core of 300+years of cumulative research and development experience in developing with ADC technology.

High-Speed Digitizer design team:

- Best in class high-speed ADC implementation
- Small footprint and low power consumption
- High measurement throughput
- ASIC design, IP and technical know-how
- Multiple OS and software environment
- Advanced firmware development



M9703A AXIe 12-Bit High-Speed Digitizer

See Events That You Could Not See Before!

Key Features

- 12 bit resolution
- **8 channels @ 1 GS/s or 1.6 GS/s** (4 ch @ 3.2 GS/s when interleaved)
- **Reach up to >100 phase-coherent channels**
- **DC to 2 GHz input frequency range**
- **DC to 1.4 GHz instantaneous BW**
- Internal Customizable FPGAs
- 1.1 GB/s data transfer

M9703A OS support

- Windows
- XP (32-bit)
- Vista (32/64-bit)
- 7 (32/64-bit)
- Linux

Drivers – MD1 software

- IVI-C, IVI-COM
- LabVIEW
- Matlab (through IVI-COM)

OTS application software

- MD1 soft front panel
- AcqirisMAQS U1092A-S01/S02/S03
- 89600 VSA software

M9703A
See Things You Were Not Able To See Before!

- 4096 quantization levels per channel (12-bit ADC)
- Very high dynamic range at GHz frequency
  - >9 effective bits
  - Very low system noise level of <500 uV rms
- Versatile attributes and exceptional channel synchronization for high signal quality and a very large input window simultaneously
  - Precise offset control
  - Excellent timing and synchronization
  - Stacking : combined window is 8,192 levels → **13-bit resolution!!!**

FRF Option Performance

Performance	Frequency	Standard	-FRF
ENOB	48 MHz 100 MHz 410 MHz 650 MHz 900 MHz	9.0 Typ 9.1 Typ 8.9 Typ (8.2 spec) Not spec'ed Not spec'ed	9.1 Typ 9.2 Typ 9.1 Typ 9.0 Typ 8.8 Typ
SNR	48 MHz 100 MHz 410 MHz 650 MHz 900 MHz	58 dB Typ 58 dB Typ 56 dB Typ (54 dB spec) Not spec'ed Not spec'ed	58 dB Typ 58 dB Typ 58 dB Typ 57 dB Typ 55 dB Typ
SFDR	48 MHz 100 MHz 410 MHz 650 MHz 900 MHz	59 dBc Typ 63 dBc Typ 60 dBc Typ (52 dBc spec) Not spec'ed Not spec'ed	60 dBc Typ 65 dBc Typ 63 dBc Typ 64 dBc Typ 61 dBc Typ