

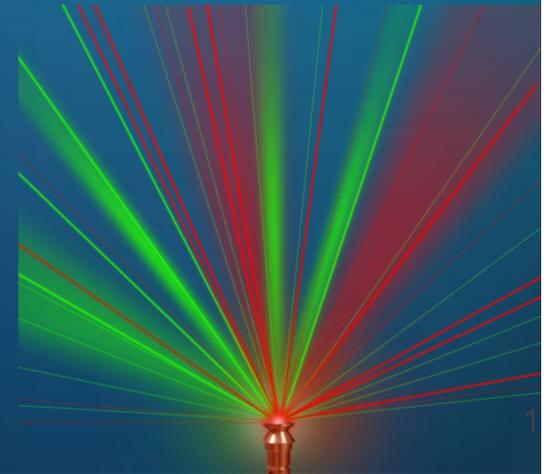
**Tektronix**

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# Enhancements in Real-Time Multi-Channel Detection Capability

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2018 PDV CONFERENCE





# Agenda

- Introduction
- Newest Generation Tek Acquisition Technology
- High/Ultra Performance O/E
- De-embedding Channel Effects

# Newest Generation Acquisition Technology

# 5 Series MSO and Low Profile

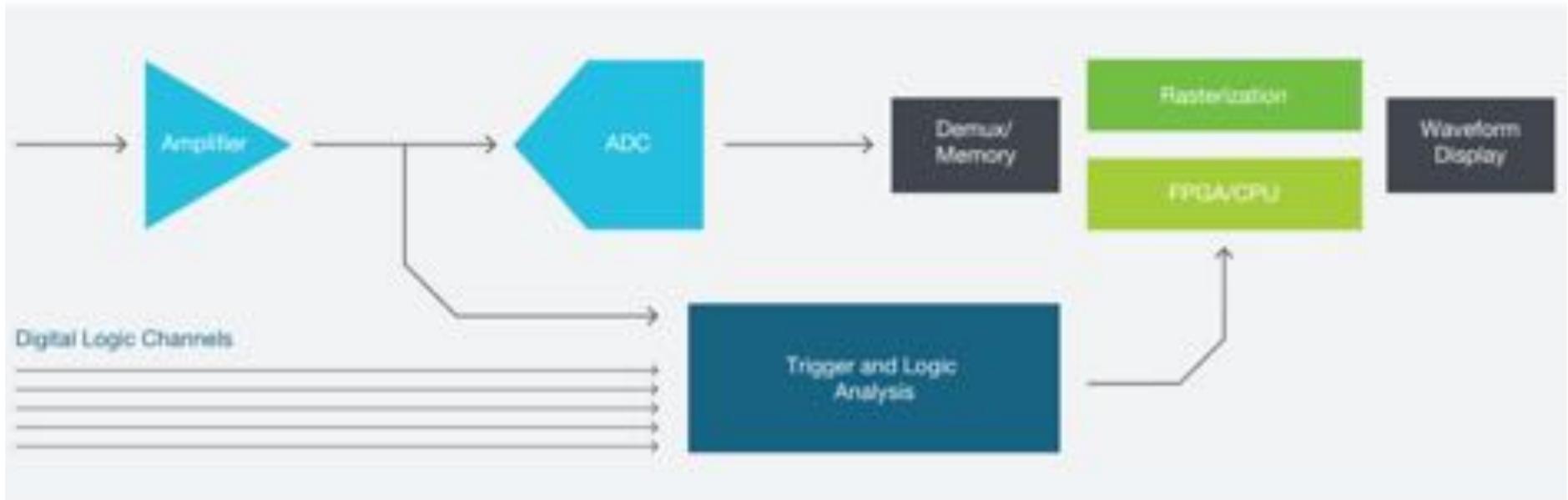
TWO FORM FACTORS, SAME GREAT PERFORMANCE

*Same high performance 12-bit oscilloscope, same programmatic command set making it easy to transition from bench to system applications*



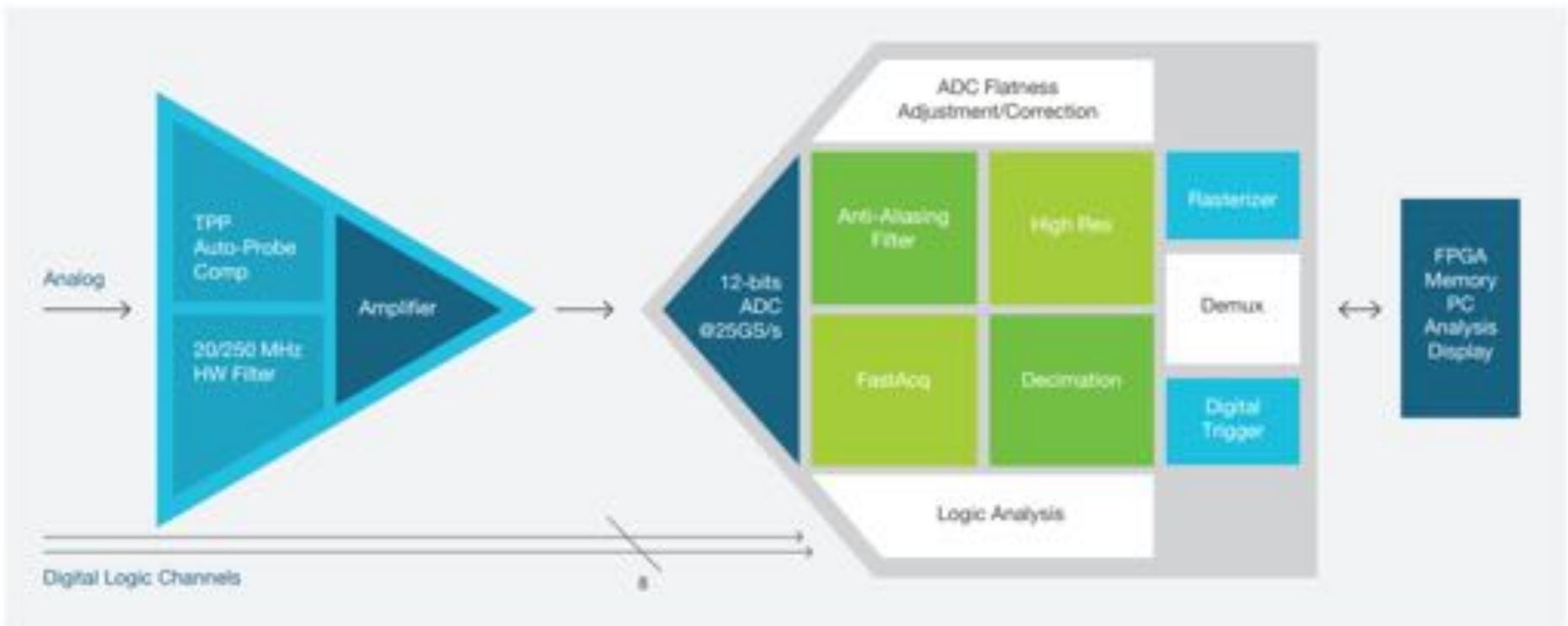
# Signal Integrity

## CONVENTIONAL OSCILLOSCOPE ARCHITECTURE



# Improved Signal Integrity

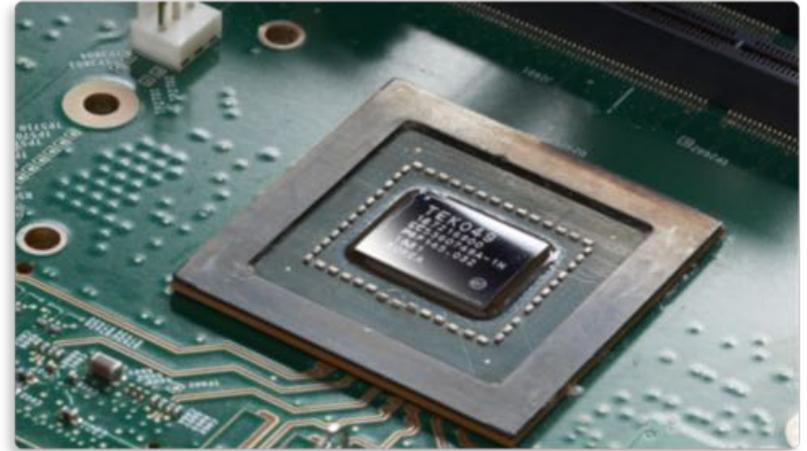
## NEW TEKTRONIX SIGNAL PATH



# Improved Signal Integrity

NEW CUSTOM TEKTRONIX ASIC TECHNOLOGY

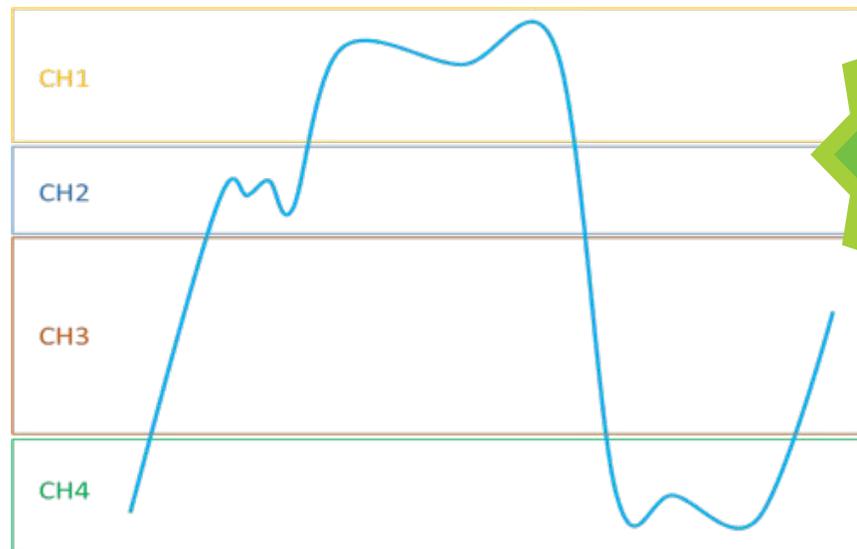
- **New** Custom Tektronix ASIC
- 25GS/s Sample Rate per chip  
**6.25GS/s per FlexChannel™ input**
- 12-bit Analog to Digital Convertor (ADC)
  - 4,096 digitizing levels **16x More Resolution over 8-bit ADCs**
- Advanced Integration in one chip
  - Trigger Circuitry ***New Digital Trigger***
  - FlexChannels (can be one analog channel or 8 digital channel)
  - Demux



# Signal Integrity

## WHY PEOPLE STITCH SIGNALS TOGETHER

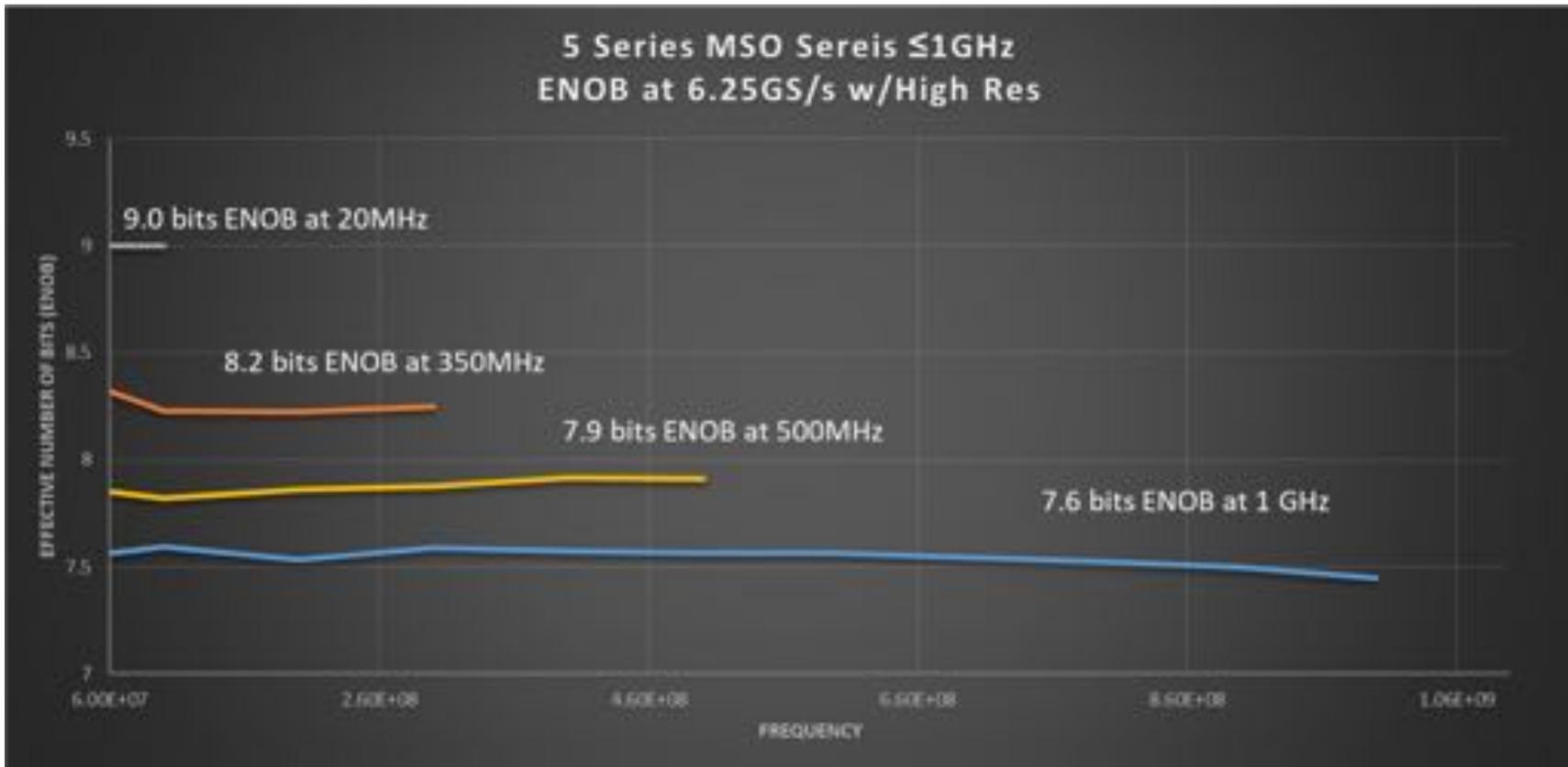
- To view small signals riding on large signals, you need high dynamic range. Traditional 8-bit scopes don't have enough, so users will often break up the signal into multiple channels.
- Using 4+ channels to capture a single signal, using different gain/ offset/ position and overdriving the input, they capture then combine the data and 'stitch' it back together



Not needed  
with 12-bit  
ADC

# Signal Integrity

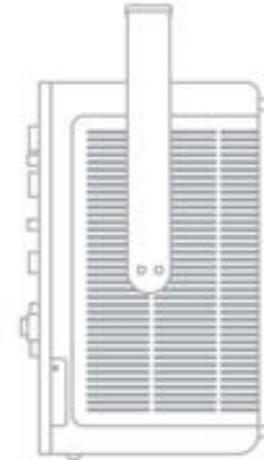
DRIVES IMPROVEMENTS IN EFFECTIVE NUMBER OF BITS (ENOB)



# Signal Integrity

## IMPROVED HORIZONTAL TIME BASE

- Clock is more accurate, designed from the Tektronix 70K-SX Series
- *Improves* Effective Number of Bits (ENOB)
- *Improves* Delta Time Accuracy (DTA)
- *Improves* Trigger functionality
- *6x Better* Sample Jitter (aperture uncertainty)
  - MSO/DPO5000B: 3ps
  - 5 Series MSO: <450fs



# Extreme Channel Density

## 5 SERIES MSO LOW PROFILE

5 Series MSO Low Profile	MSO58LP
Bandwidth	1 GHz
Maximum Analog Channels / Digital Channels	8 Analog / 64 (op. in blocks of 8)
Sample Rate (all Analog or Digital )	6.25 GS/s
Standard Record Length (all A&D ch.)	125 Mpts
Waveform Capture Rate	> 500,000 wfms/s
ADC Resolution	12 bits
Effective Number of Bits (ENOB)	7.6 bits @ 1 GHz with High Res
Aux Trig Input	$\pm 5$ Vrms, 50 $\Omega$ SMA
Arbitrary/Function Generator	Up to 50 MHz (opt.)
Operating System	Closed Linux
System Programming Integration Tools	MATLAB, NI LabVIEW, IVI-C, IVI-COM, LXI, Python and more
Remote Access	Easy Internet Browser Access
Dimensions (Height)	3.44 inches (2U Rack)



*The 5 Series MSO low profile provides best combination of channel density, performance, and cost per channel providing deeper insights in less space*

# High / Ultra Performance O/E

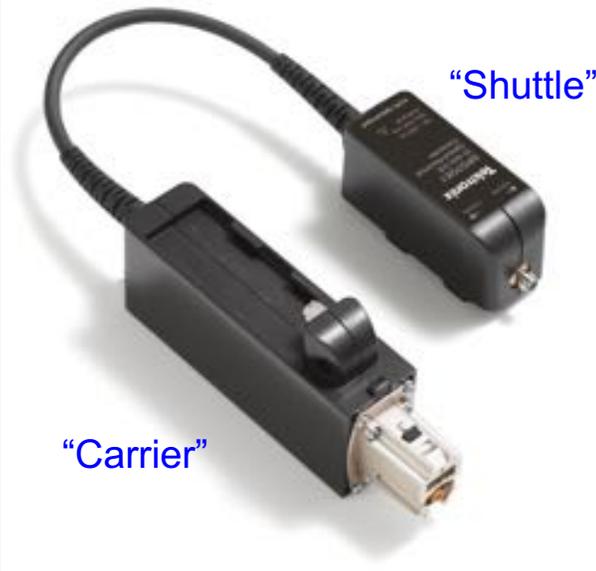
# Calibrated O/E

## DPO70E1 AND DPO70E2

- Broad wavelength O/E 750nm – 1650nm
- 33GHz/59GHz electrical bandwidth
- Single mode, multi-mode,
- Compatible with TekConnect and ATI inputs
- Use with DPO/MSO70kC/D/DX and DPO70kSX models



TekConnect – 33 GHz O/E



“Carrier”

“Shuttle”



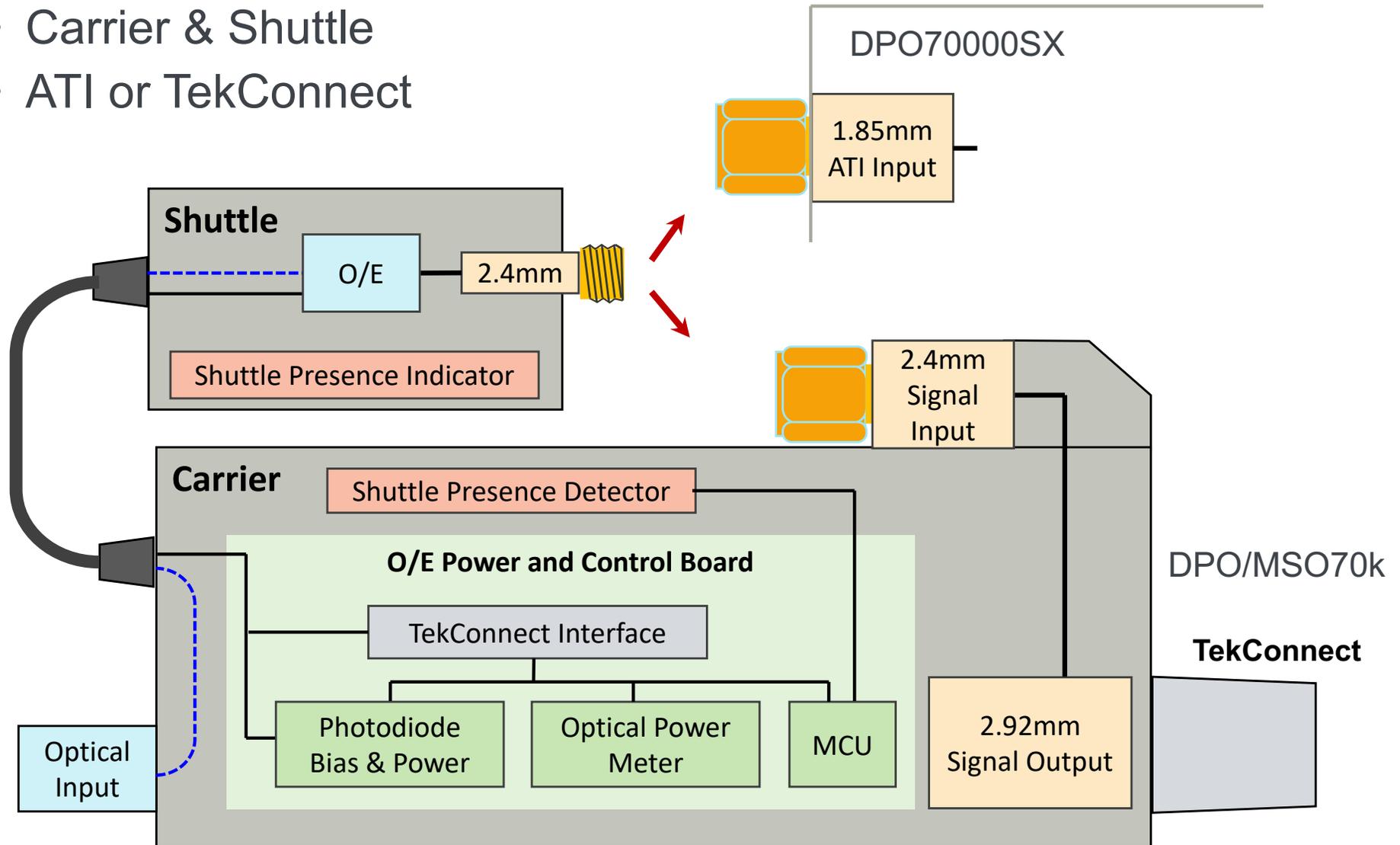
ATI – Mechanical support deck

# O/E Key Specs

Feature / Function	DPO70E1		DPO70E2	
Connector Type	FC/PC & FC/APC		FC/PC & FC/APC	
Input Fiber Type and Diameter	FC/PC: 50 $\mu$ m (SMF and MMF compatible) FC/APC: 9 $\mu$ m (SMF compatible)		FC/PC: 9 $\mu$ m (SMF compatible) FC/APC: 9 $\mu$ m (SMF compatible)	
Wavelength Range	750 nm – 1650 nm (Opt FC/PC) 1260 nm – 1650 nm (Opt FC/APC)		1200 nm to 1650 nm (Opt FC/PC) 1200 nm to 1650 nm (Opt FC/APC)	
Calibrated Wavelengths	850 nm, 1310 nm, 1550 nm (Opt FC/PC) 1310 nm, 1550 nm (Opt FC/APC)		1310 nm, 1550 nm (Opt FC/PC) 1310 nm, 1550 nm (Opt FC/APC)	
Electrical Bandwidth	33GHz		59GHz	
Coupling	DC		DC	
Risetime (10-90%, typical)	10.2ps		8ps	
RMS Optical Noise (1310 nm)	Typical	Max	Typical	Max
Raw O/E Response - (TekConnect / ATI)	7.42uW / 9.31uW	8.83uW / 9.93uW	11uW / 16uW	13uW / 18uW
Flat to 33Ghz Response - (TekConnect / ATI)	10.6uW / 9.84uW	12.71uW / 12.31uW	11uW / 16uW	13uW / 18uW
Max Input Power - typical (linear / non-destruct)	4 mW / 8 mW		2mW / 4mW	
Operating Temperature	10 <sup>0</sup> C to 40 <sup>0</sup> C		10 <sup>0</sup> C to 40 <sup>0</sup> C	

# DPO70E1 Block Diagram

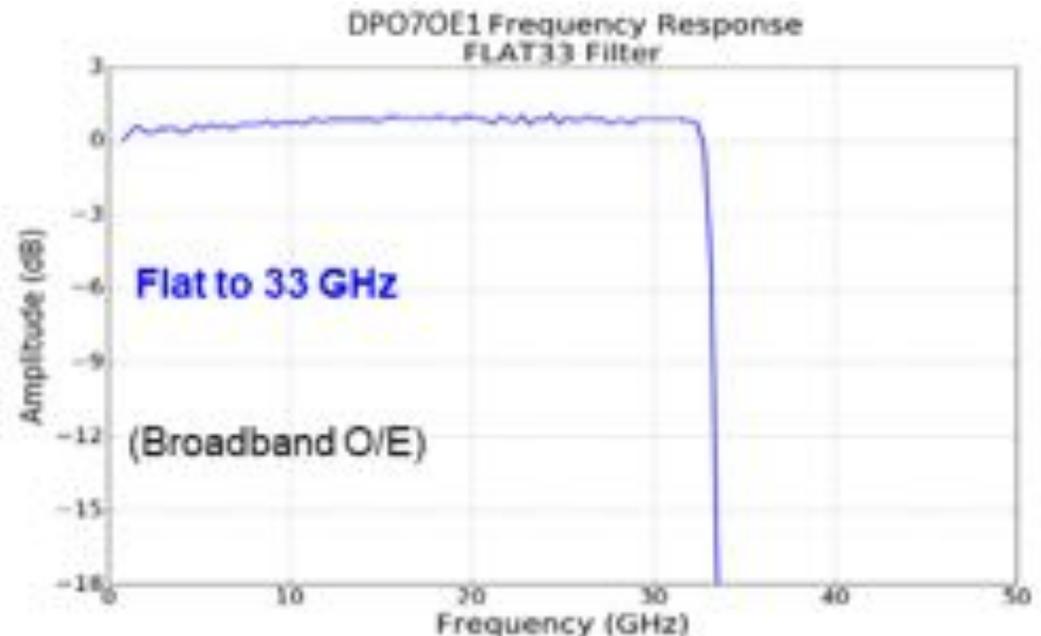
- Carrier & Shuttle
- ATI or TekConnect



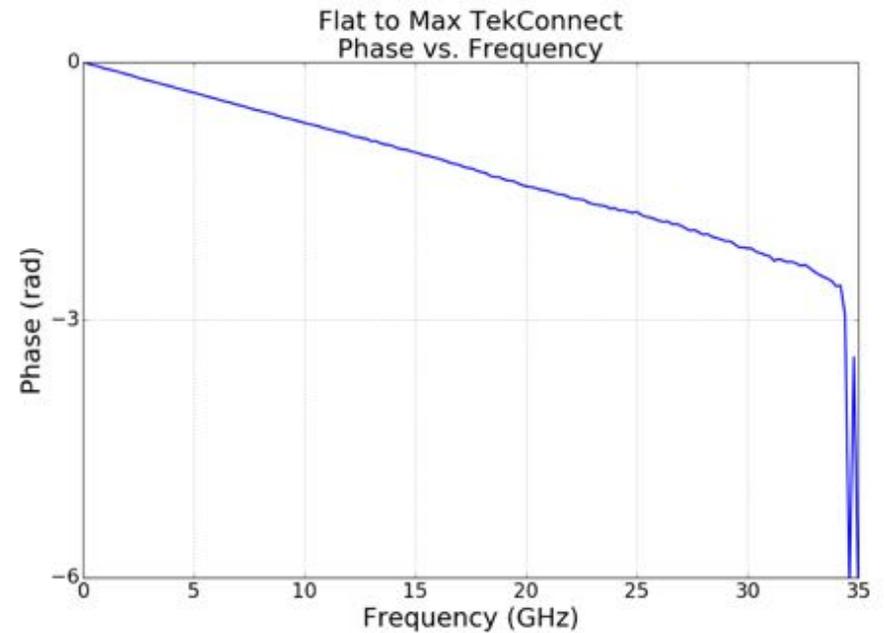
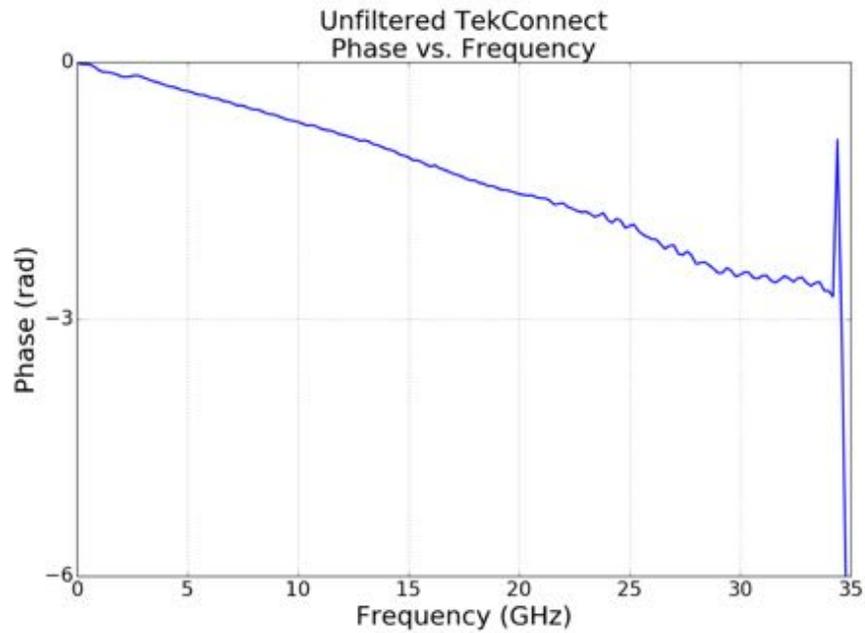
# DPO70E1 – Frequency Response Selection

## SELECTABLE FILTER

- Frequency Response
  - Unfiltered O/E response
  - Flat to 33GHz, sharp roll-off

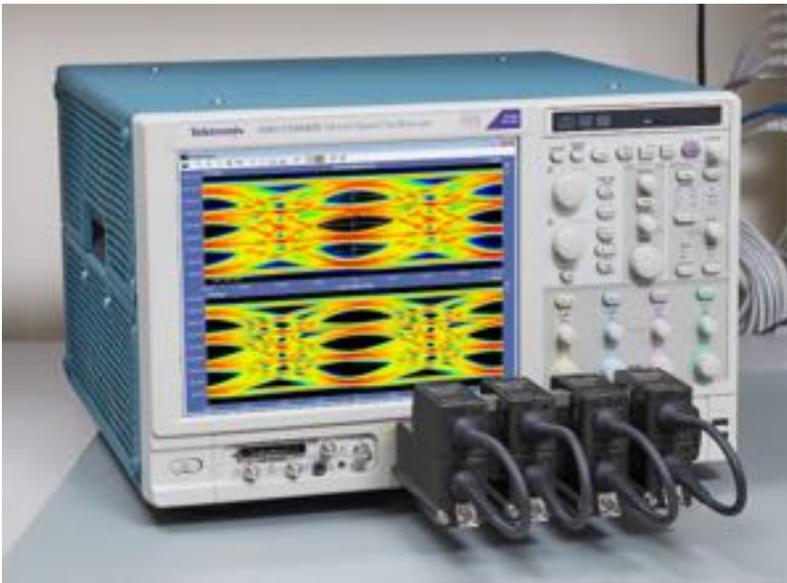
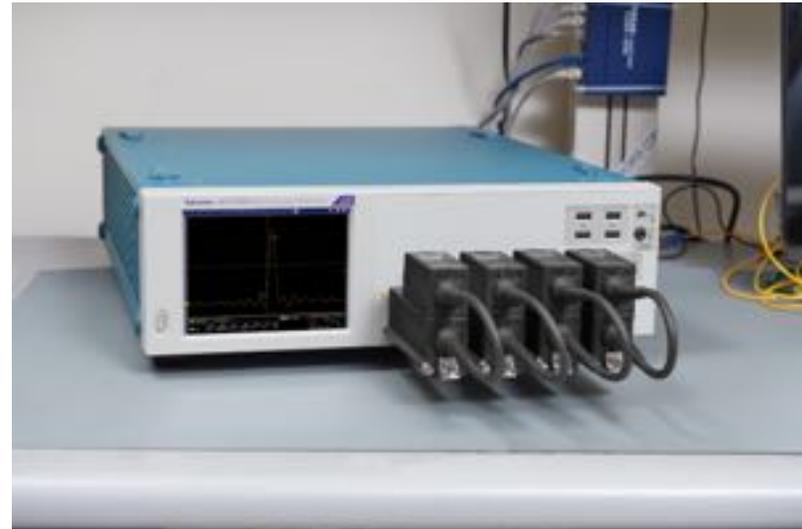


# DPO70E1 Phase Response

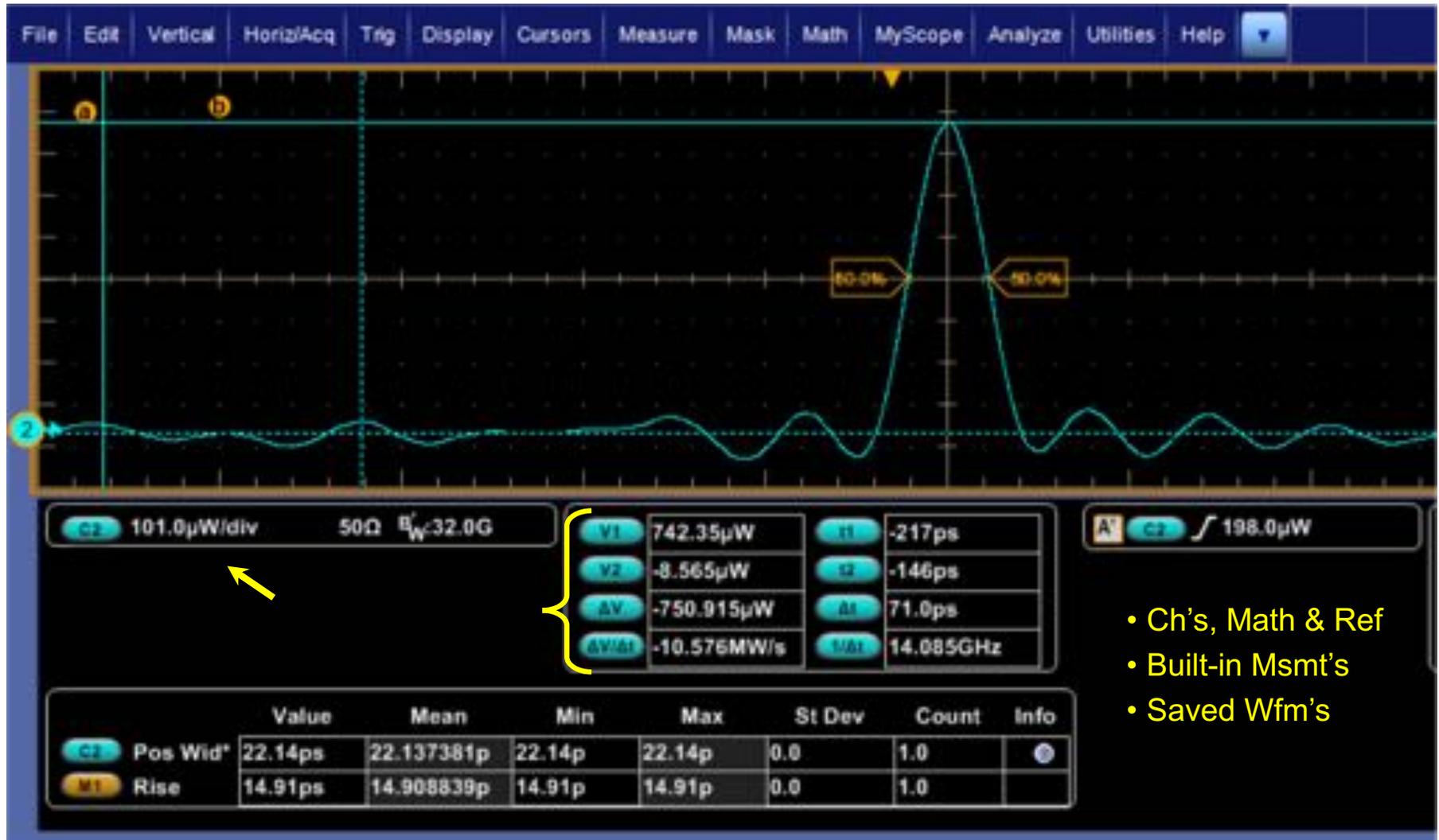


# O/E Configurations

MSO/DPO70KC/D/DX AND DPO70KSX - ATI OR TEKCONNECT



# DPO70E1 – Optical Power Scaled in Watts



- Ch's, Math & Ref
- Built-in Msmt's
- Saved Wfm's

# DPO70E1 / DPO70E2 – Control Panel



# De-embedding Channel Effects

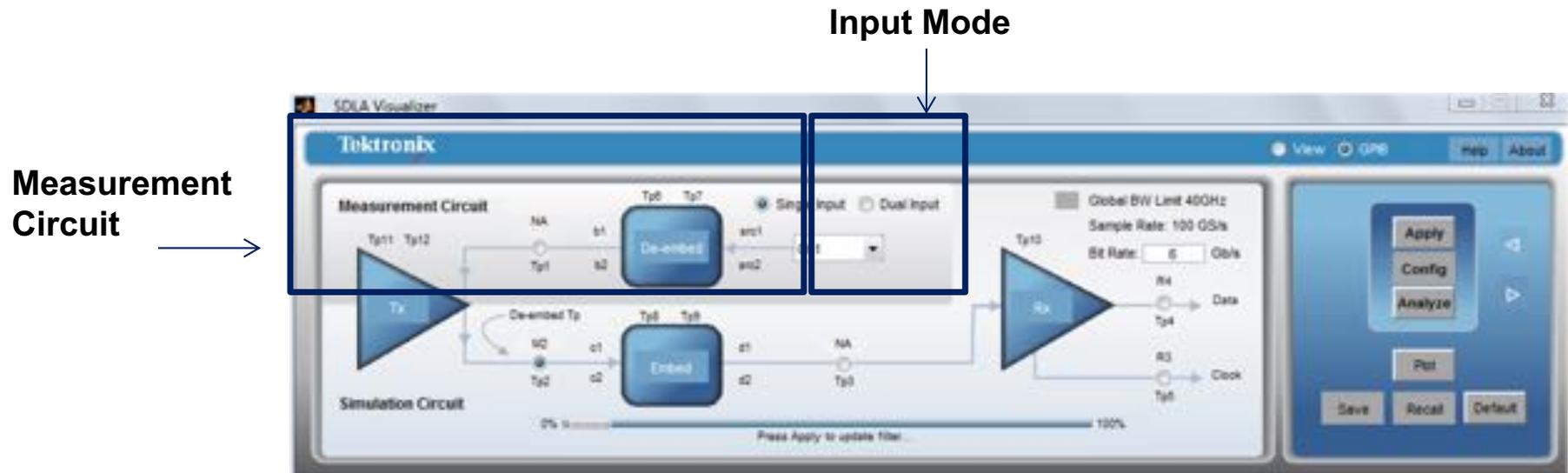


# De-embedding Channel Effects

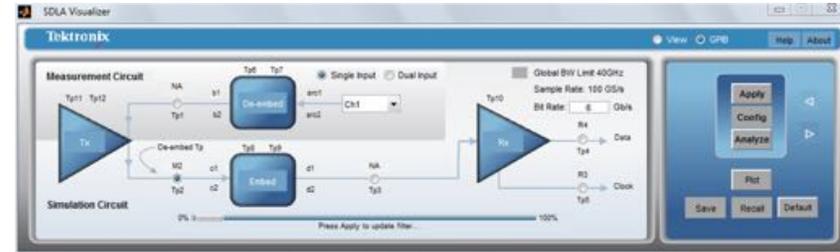
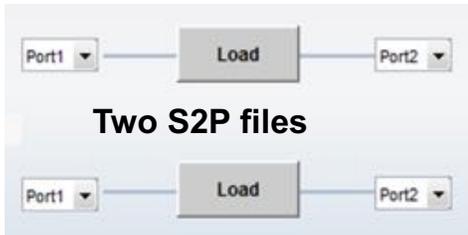
- **Methods for Insertion Loss Correction Only**
  - Precomp (AWG and Scope)
  - Tek SignalCorrect
- **Method for Insertion Loss and Reflection Correction**
  - SDLA Visualizer
    - Originally created to correct serial data channels
    - Can be used with a variety of applications
    - Robust multi-port S-parameter de-embed environment
    - Requires S-parameter data for best results (typically from VNA)
    - Preserves original acquired data
    - Provides corrected signal as a Math Waveform

# SDLA Basic Channel Model

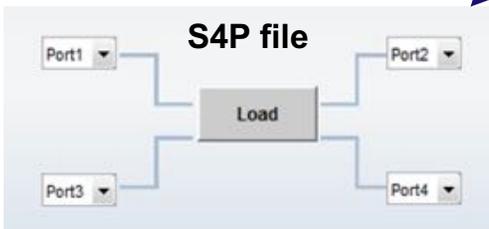
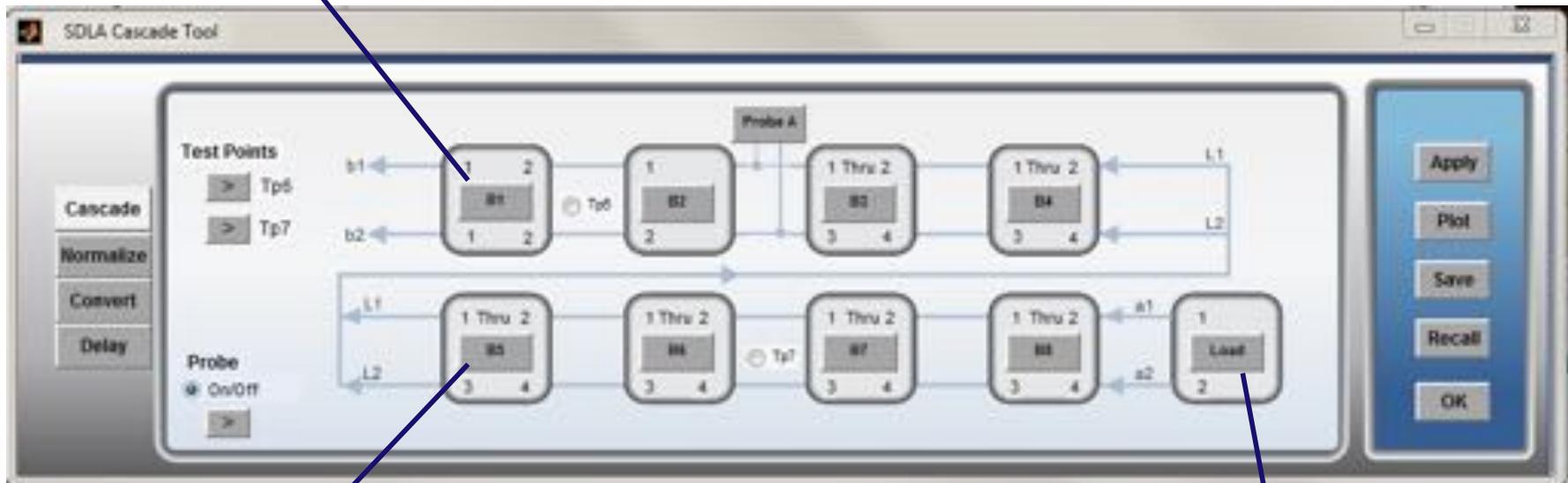
- Elements applicable to PDV work
  - Measurement Circuit De-embed (includes Scope S11)
  - Transmit Circuit (includes O/E S22)



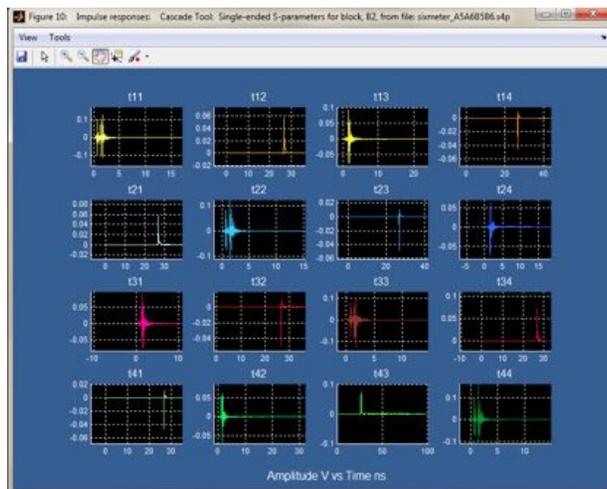
# Configuration Options for De-Embed Block



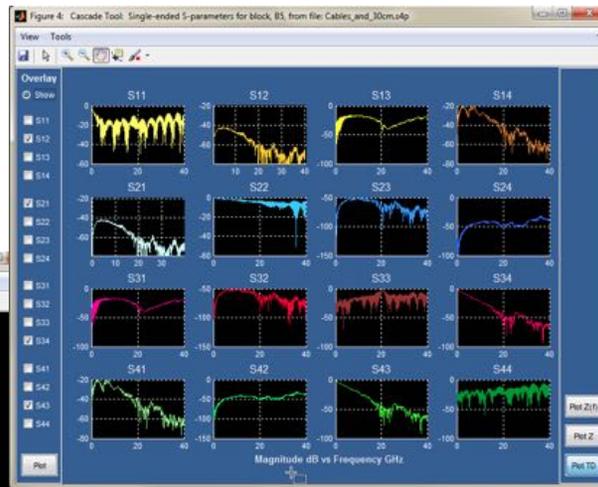
Or Two Transfer function files  
Or Two FIR files



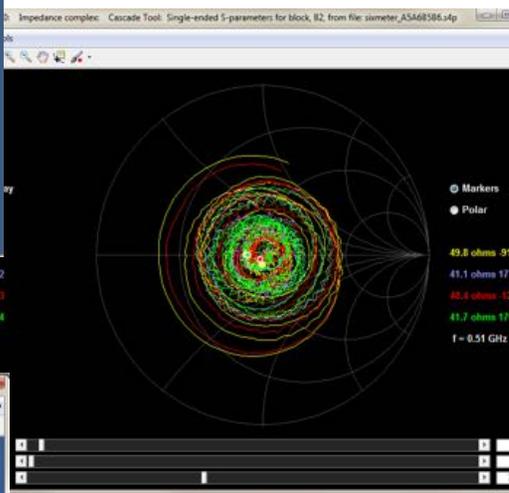
# Plot Options for De-Embed and Embed Block Elements



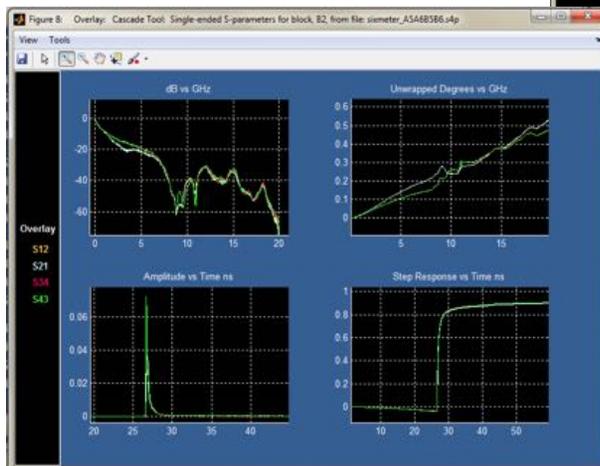
**Impulse Response  
Time Domain**



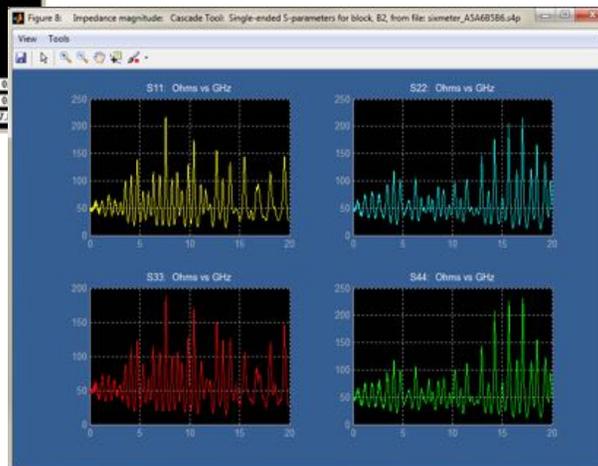
**16 S-Parameters  
Frequency Domain**



**Smith Chart**

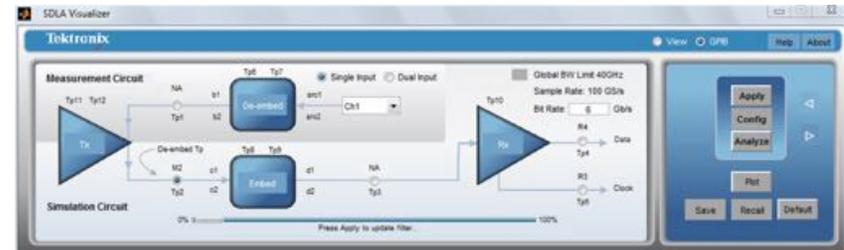


**Magnitude, Amplitude, Step Response**



**Impedance vs. Frequency**

# Configuration for Transmitter Block



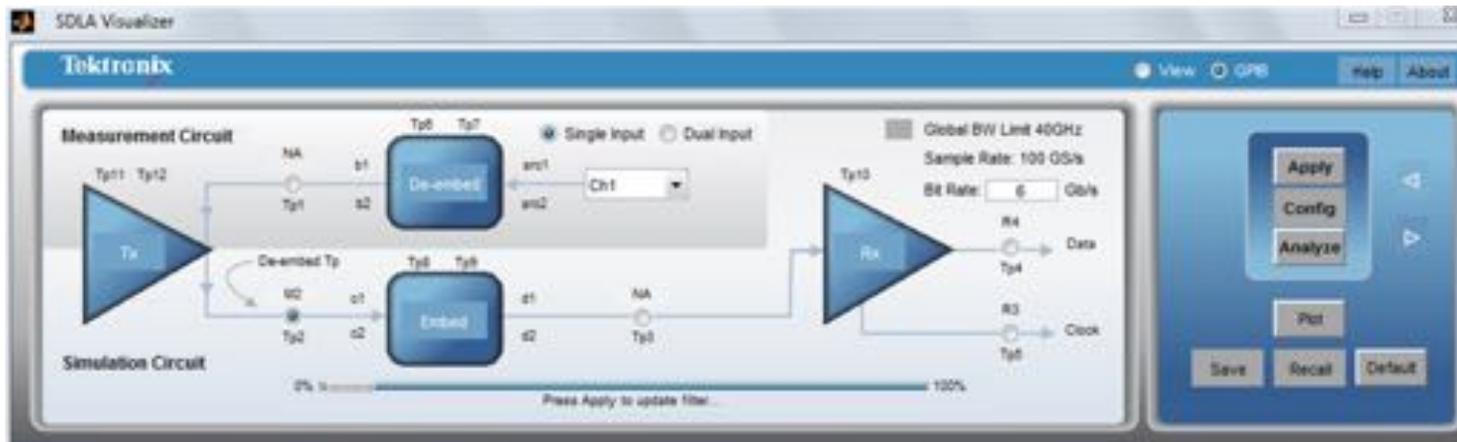
- O/E S22 is entered into the Transmitter Block

Measurement Circuit →



# Final Steps

- Once the Transmitter and Measurement blocks have been defined, the remaining step is to build the correction filter and apply it to the waveform data
  - Apply button builds the FIR filter
  - Analyze button applies the filter to the waveform data to correct signal
  - Corrected signal is displayed in specified Math channel





# Uses of SDLA Visualizer

- High Speed Serial testing – compensating for cable and fixture losses, as well as reflections, resulting in larger eye opening and lower measured jitter. Visualizing and measuring signals that may be impossible to access directly with a probe.
- Coherent Optical test – removing reflections between O/E and Scope Input
- SATCOM test – removing losses, phase shift, and reflections that degrade EVM measurements. Includes de-embedding waveguides

# Tektronix

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